

# Latitude3000 Schematic

## Haswell-ULT

2013-4-19  
REV : X01

***DY : None Installed***  
***UMA: UMA only installed***  
***OPS: DISCRTE OPTIMUS installed***

<Core Design>



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Title

**Cover Page**

Size  
A3

Document Number

**Latitude300 Haswell**

Rev

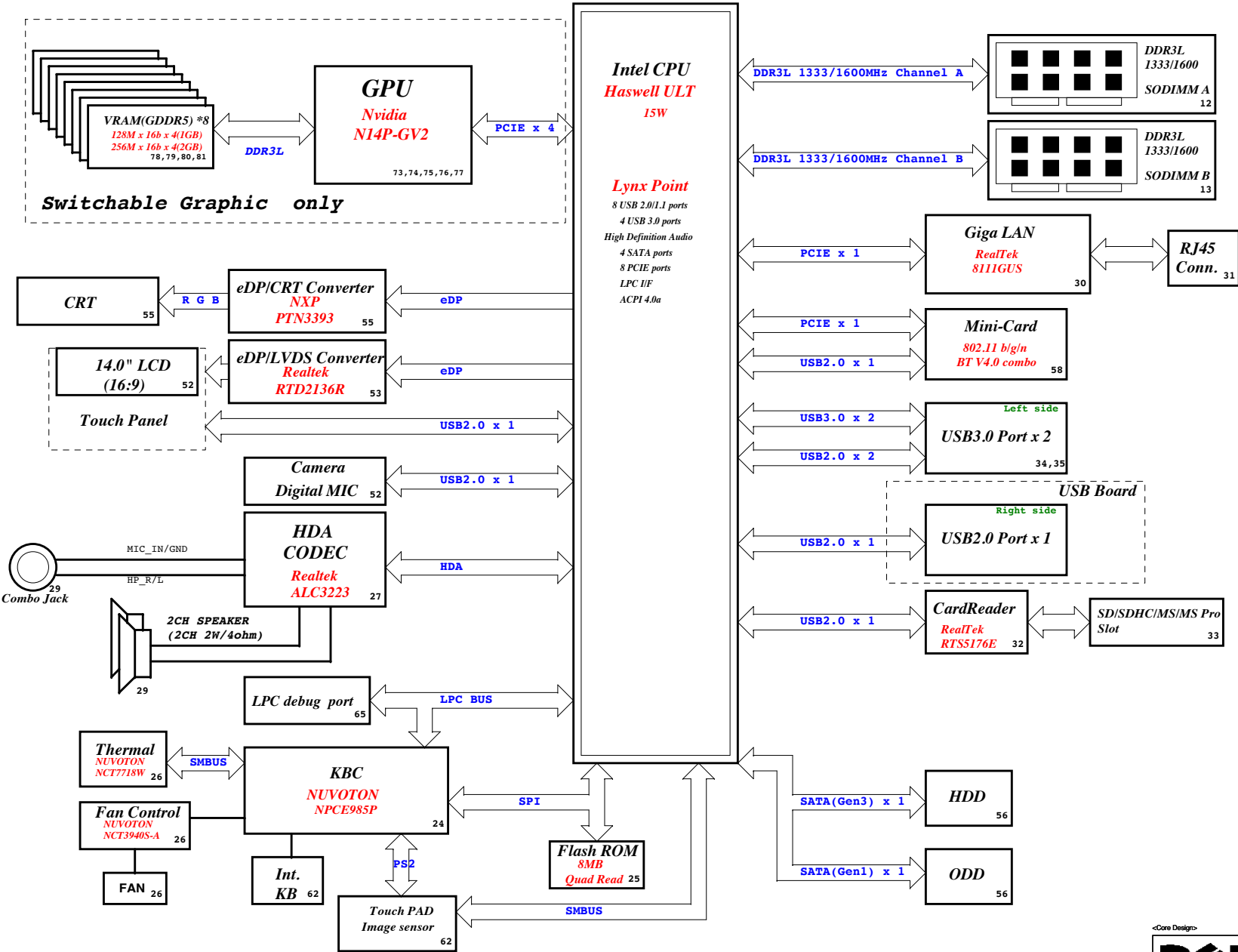
**X00**

Date: Friday, April 19, 2013

Sheet 1 of 104

Project code: 91.46001.001  
PCB P/N : 13221-SB  
Revision: X01


Latitude3000 Block Diagram



|   |  |       |
|---|--|-------|
| CHARGER   |  | 44    |
| BQ24717   |  |       |
| INPUTS  | OUTPUTS  |       |
| AD+   | DCBATOUT   |       |
| BT+   |  |       |
| SYSTEM DC/DC  |  | 45    |
| TPS51225  |  |       |
| INPUTS  | OUTPUTS  |       |
| DCBATOUT  | 3D3V_AUX_S5<br>5V_AUX_S5<br>5V_S5<br>3D3V_S5   |       |
| CPU Core Power                                      |  | 46,47 |
| ISL95813  |  |       |
| INPUTS  | OUTPUTS  |       |
| DCBATOUT  | VCC_CORE   |       |
| DDR3L SUS   |  | 49    |
| TPS51216  |  |       |
| INPUTS  | OUTPUTS  |       |
| DCBATOUT  | 1D35V_S3<br>0D65V_S0   |       |
| CPU 1.05V   |  | 48    |
| RT8237  |  |       |
| INPUTS  | OUTPUTS  |       |
| DCBATOUT  | 1D05V_S0   |       |
| CPU 1D5V_S0   |  | 51    |
| TLV70215  |  |       |
| INPUTS  | OUTPUTS  |       |
| 3D3V_S5   | 1D5V_S0  |       |
| Switches  |  | 36 83 |
| INPUTS  | OUTPUTS  |       |
| 1D35V_S3<br>5V_S5<br>3D3V_S5<br>VCCP_CPU<br>3D3V_S0 | 1D35V_S0<br>5V_S0<br>0D675V_S0<br>3D3V_S0<br>1D05V_VGA_S0<br>3D3V_VGA_S0<br>1D35V_VGA_S0 |       |
| PCB LAYER   |  |       |
| L1:Top<br>L2:GND<br>L3:Signal<br>L4:Signal          | L5:VCC<br>L6:Signal<br>L7:GND<br>L8:Bottom   |       |

(Blanking)

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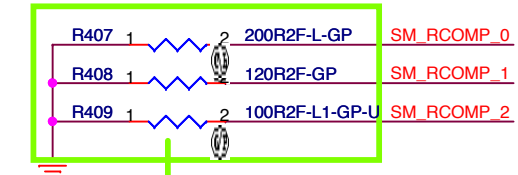
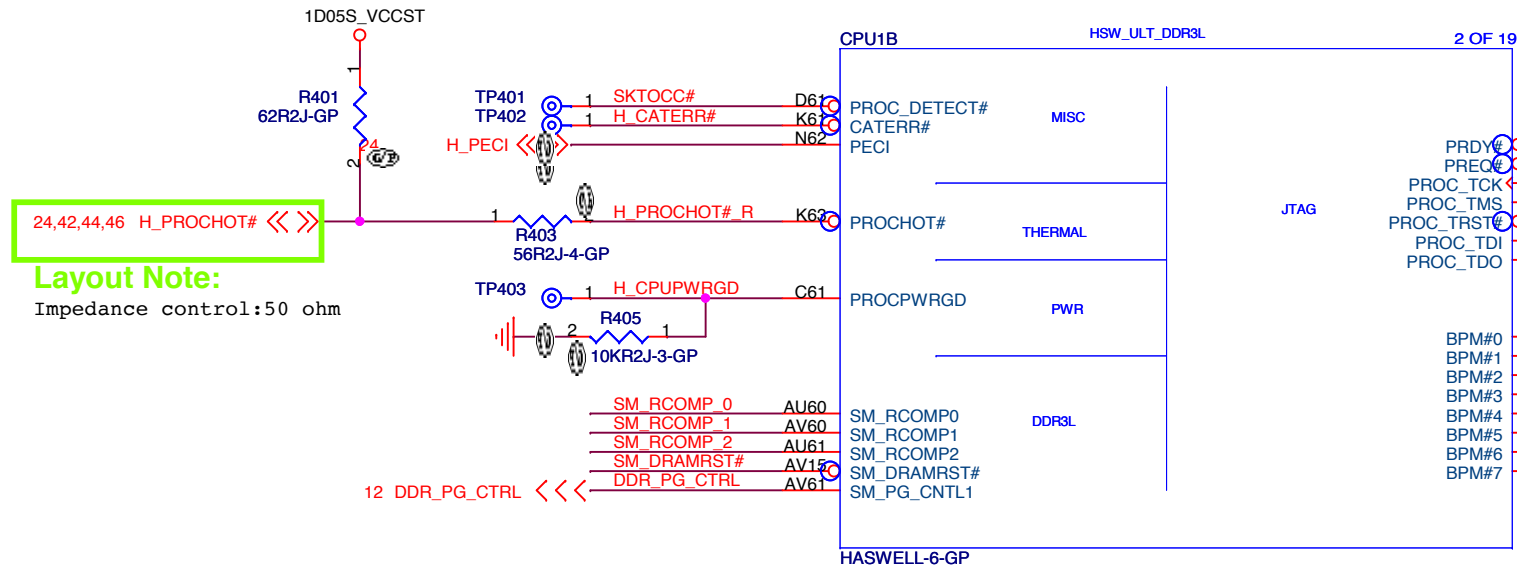
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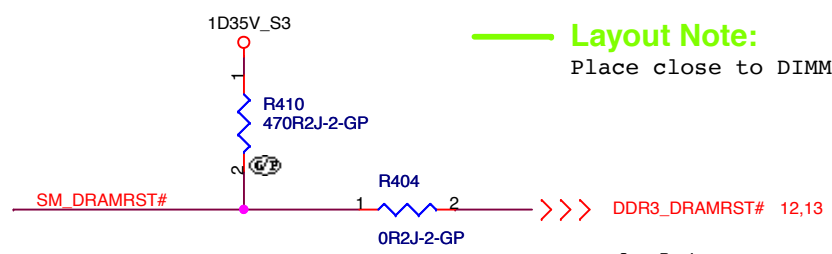
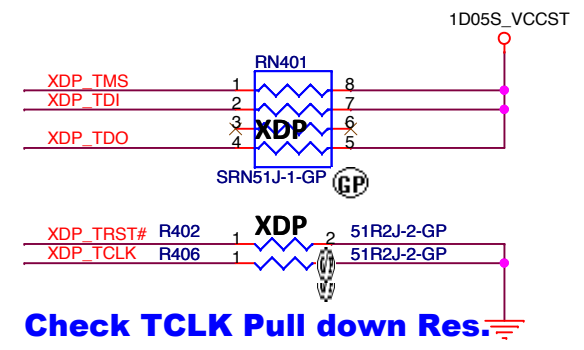
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|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                |
|-------------------------------|----------------|
| Date: Tuesday, March 26, 2013 | Sheet 3 of 104 |
|-------------------------------|----------------|

SSID = CPU




**Layout Note:**  
Design Guideline:  
SM\_RCOMP keep routing length less than 500 mils.



**Layout Note:**  
Place close to DIMM

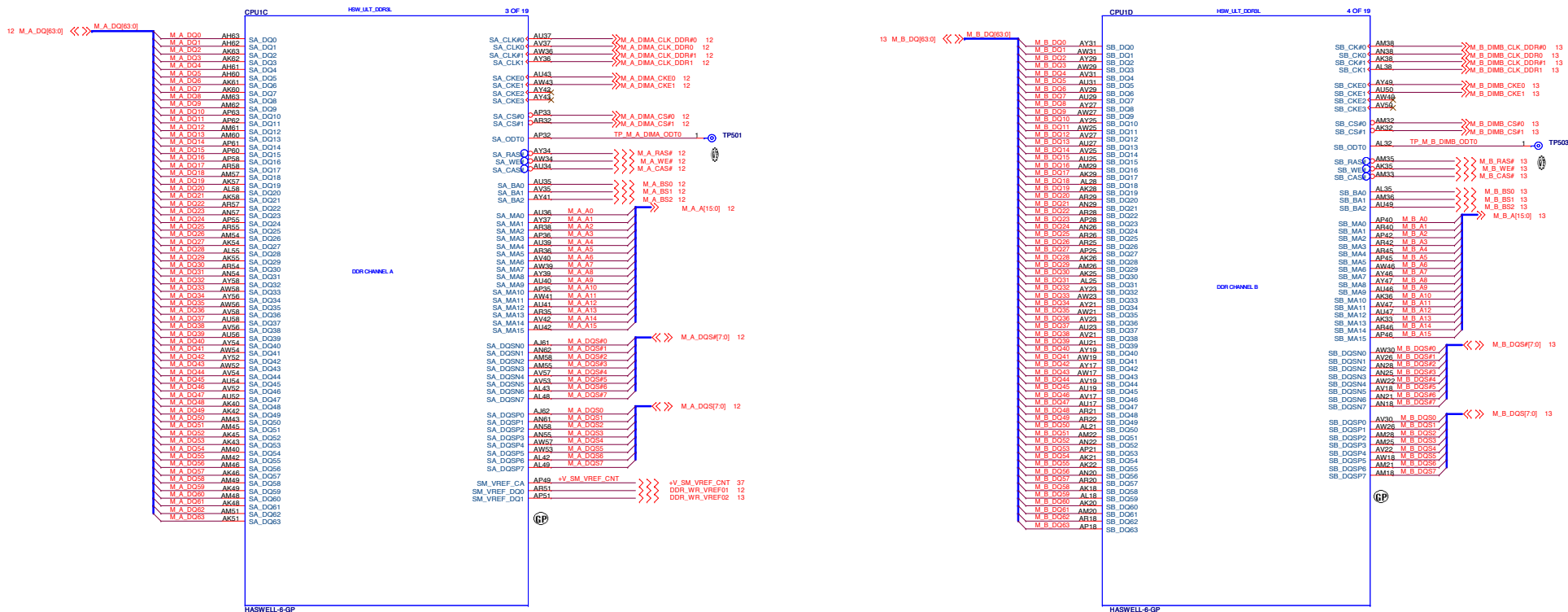
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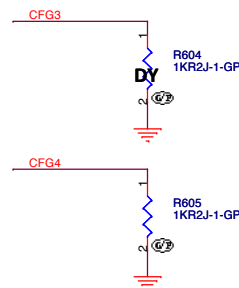
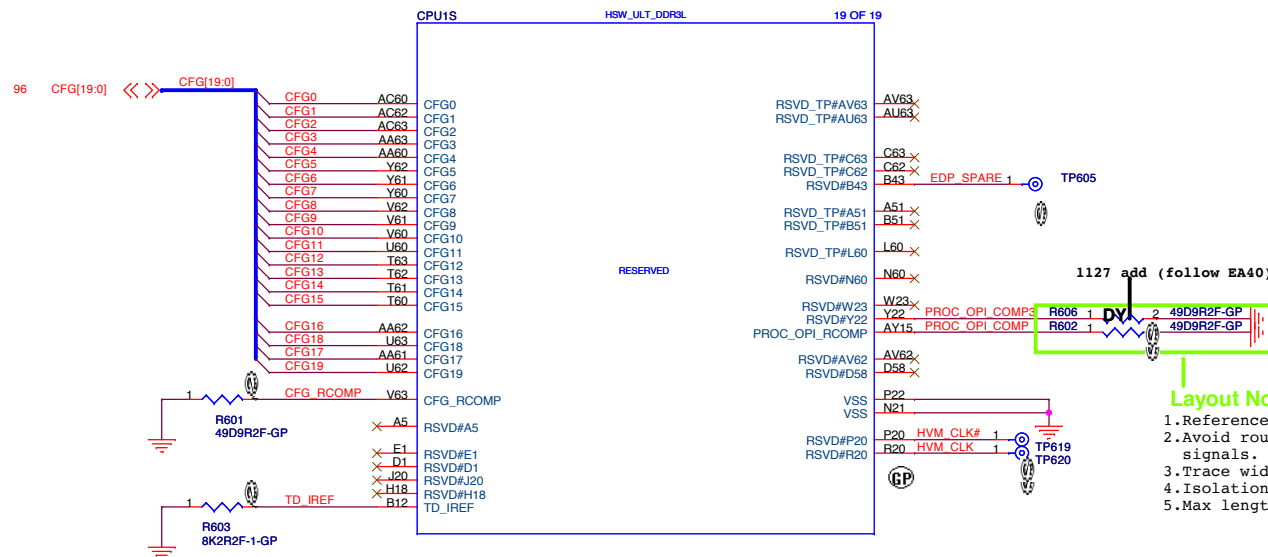
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|                                       |   |                   |
|---------------------------------------|---|-------------------|
| Title<br><b>CPU (THERMAL/MISC/PM)</b> |   |                   |
| Size<br>A4                            | Document Number<br><b>Latitude300 Haswell</b> | Rev<br><b>X00</b> |
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SSID = CPU



SSID = CPU



| PHYSICAL_DEBUG_ENABLED (DFX PRIVACY) |   |
|--------------------------------------|---|
| CFG[3]                               | 0 : ENABLED<br>SET DFX ENABLED BIT IN DEBUG INTERFACE MSR<br>1 : DISABLED |

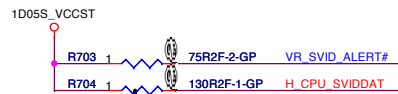
| DISPLAY PORT PRESENCE STRAP |  |
|-----------------------------|--|
| CFG[4]                      | 0 : ENABLED<br>AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT<br>1 : DISABLED<br>NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT |

<Core Design>



|                              |                 |       |                |
|------------------------------|-----------------|-------|----------------|
| Title                        |                 |       | CPU (RESERVED) |
| Size                         | Document Number | Rev   |                |
| A3                           |                 | X00   |                |
| Date: Friday, April 19, 2013 |                 | Sheet | 6 of 104       |

SSID = CPU

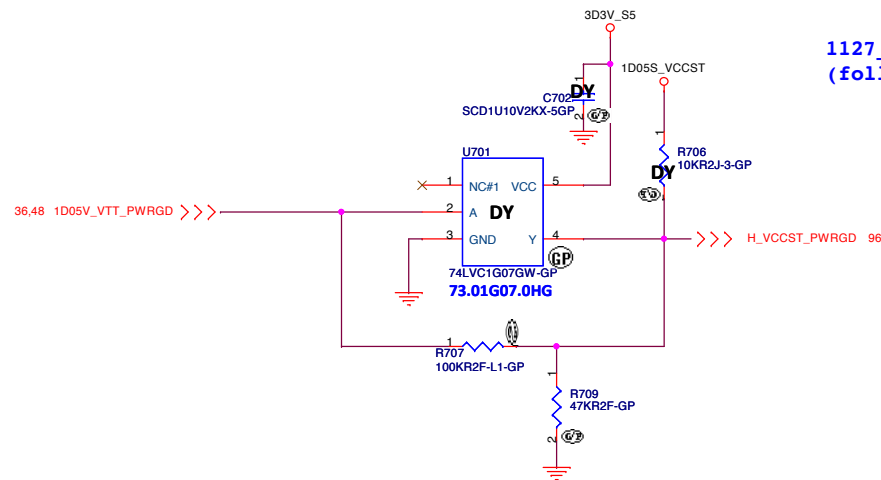


1127 130R change to 110R  
1203 110R change to 130R

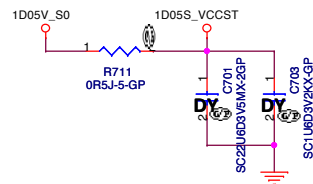
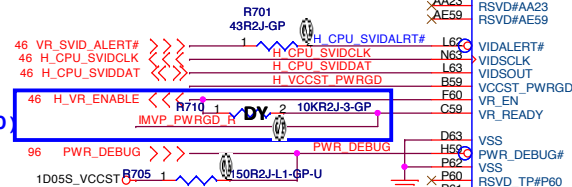
1127 Change net name of R703.2  
from VR\_SVID\_ALERT# to  
H\_CPU\_SVIDALRT#

**Layout Note:**

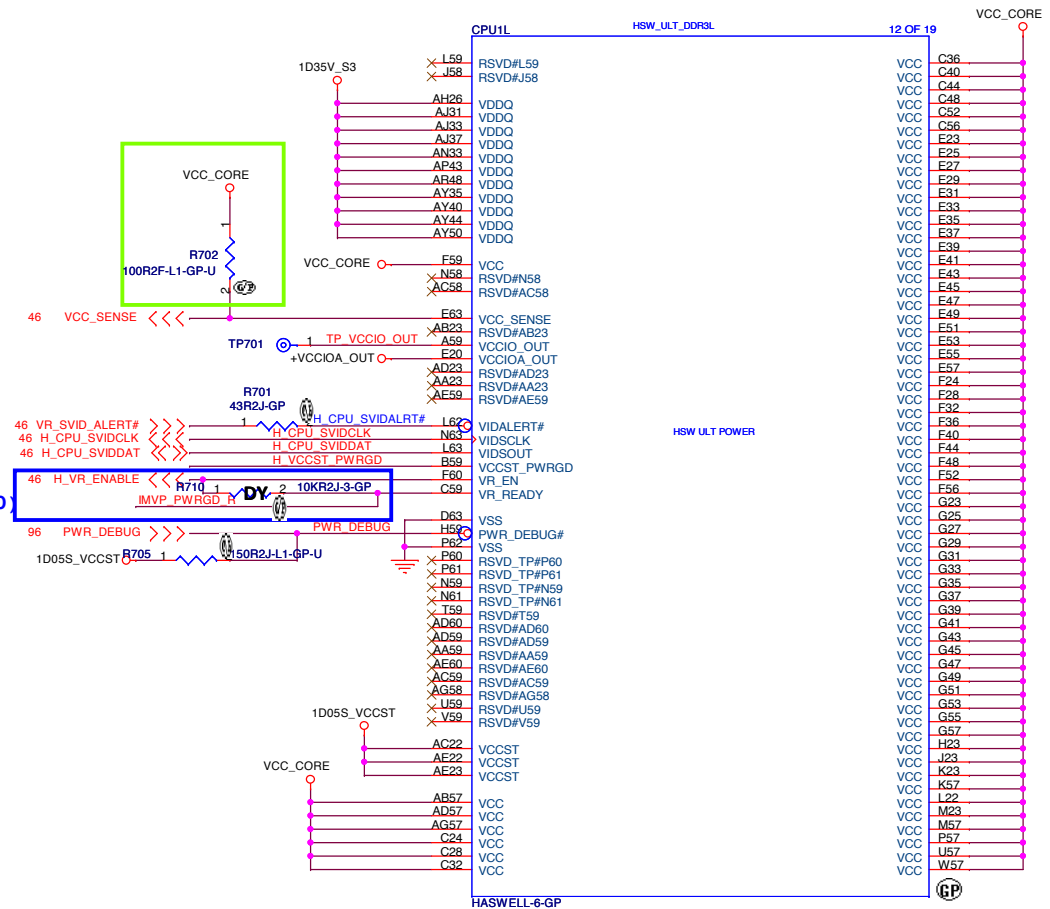
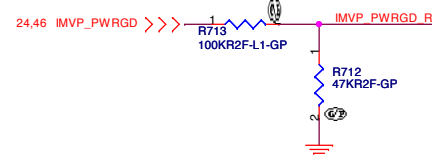
1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
3. Lwnlth match<25mil



1127 modify  
(follow EA40)



**1205 Add**



<Core Design>

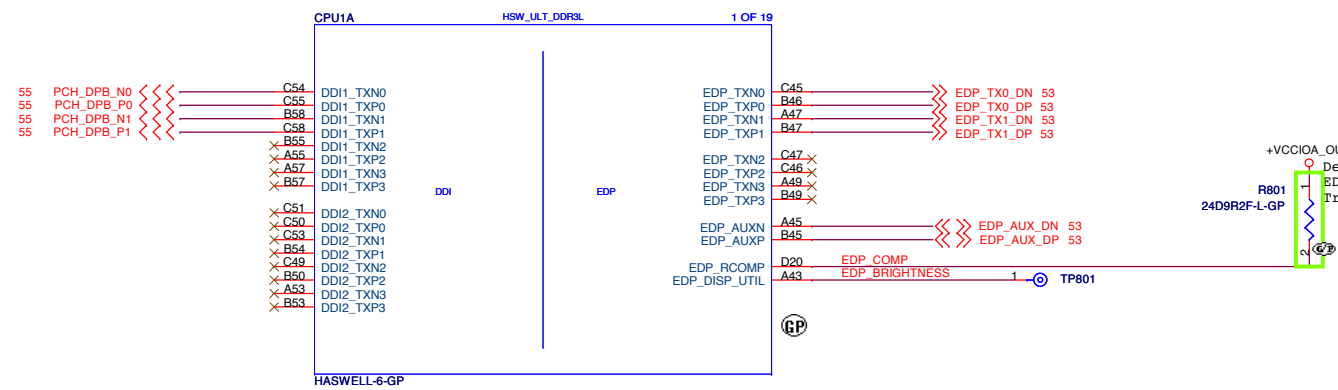


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|       |                        |       |                |
|-------|------------------------|-------|----------------|
| Title |                        |       | CPU (VCC CORE) |
| Size  | Document Number        |       | Rev            |
| A3    |                        |       | X00            |
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SSID = CPU

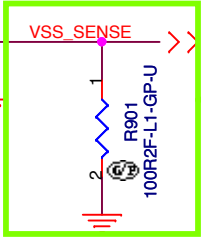
CRT



+VCCIOA\_OUT  
Design Guideline:  
EDP\_COMP keep routing length max 100 mils.  
Trace Width:20 mils.



**SSID = CPU**



## Layout Note:

1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE  
impedance=50 ohm
3. Lwngth match<25mil

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Title

**CPU (VSS)**

Size  
A4

Document Number

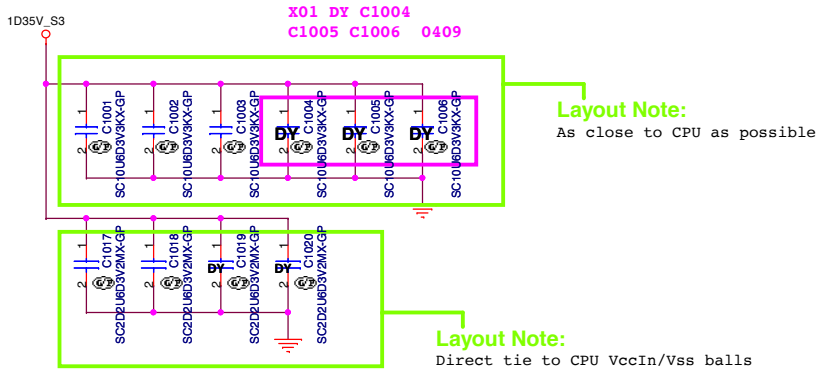
## Latitude300 Haswell

Rev  
**X00**

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SSID = CPU



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Title

**Reserved**

Size

A3

Document Number

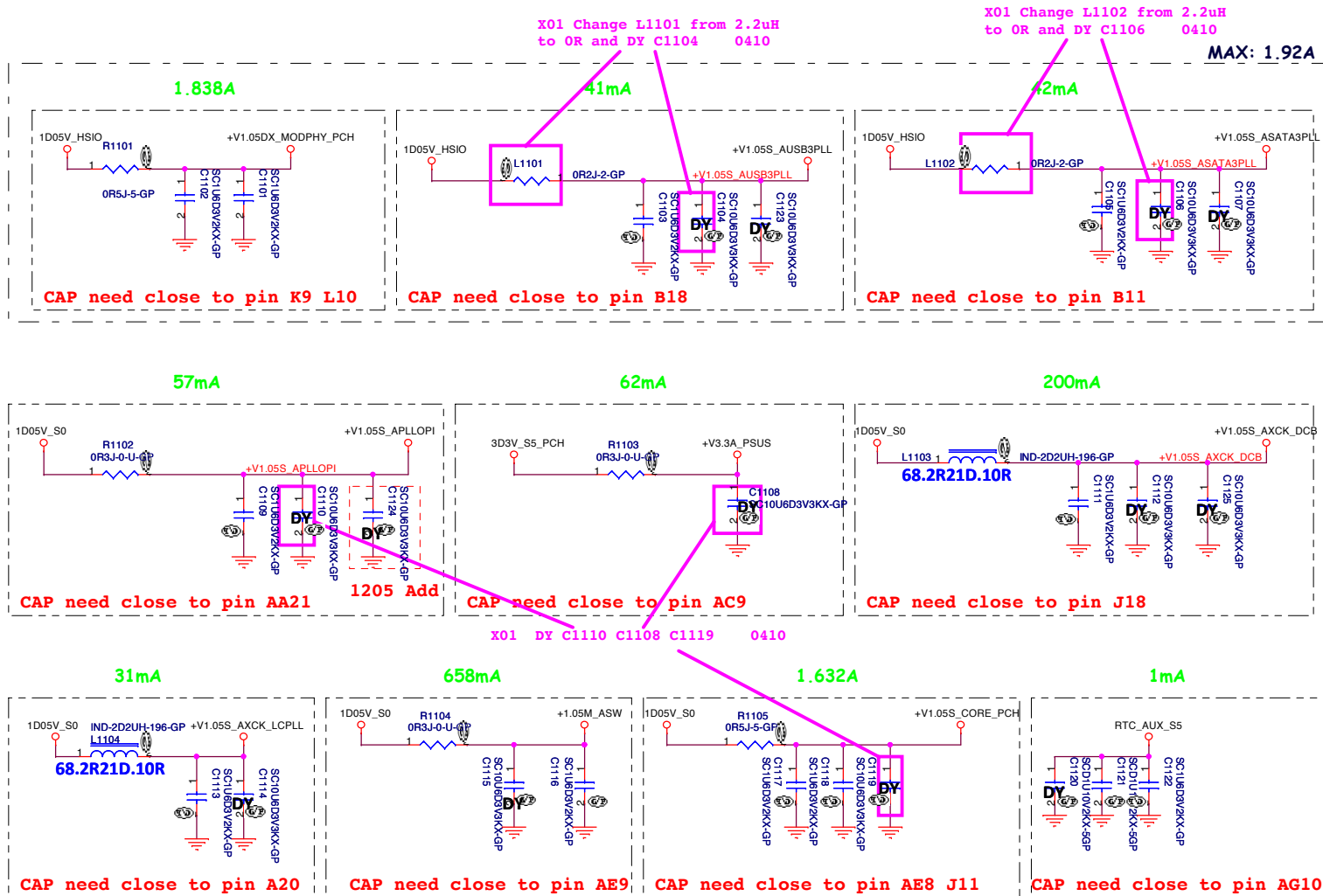
**Latitude300 Haswell**

Rev

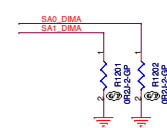
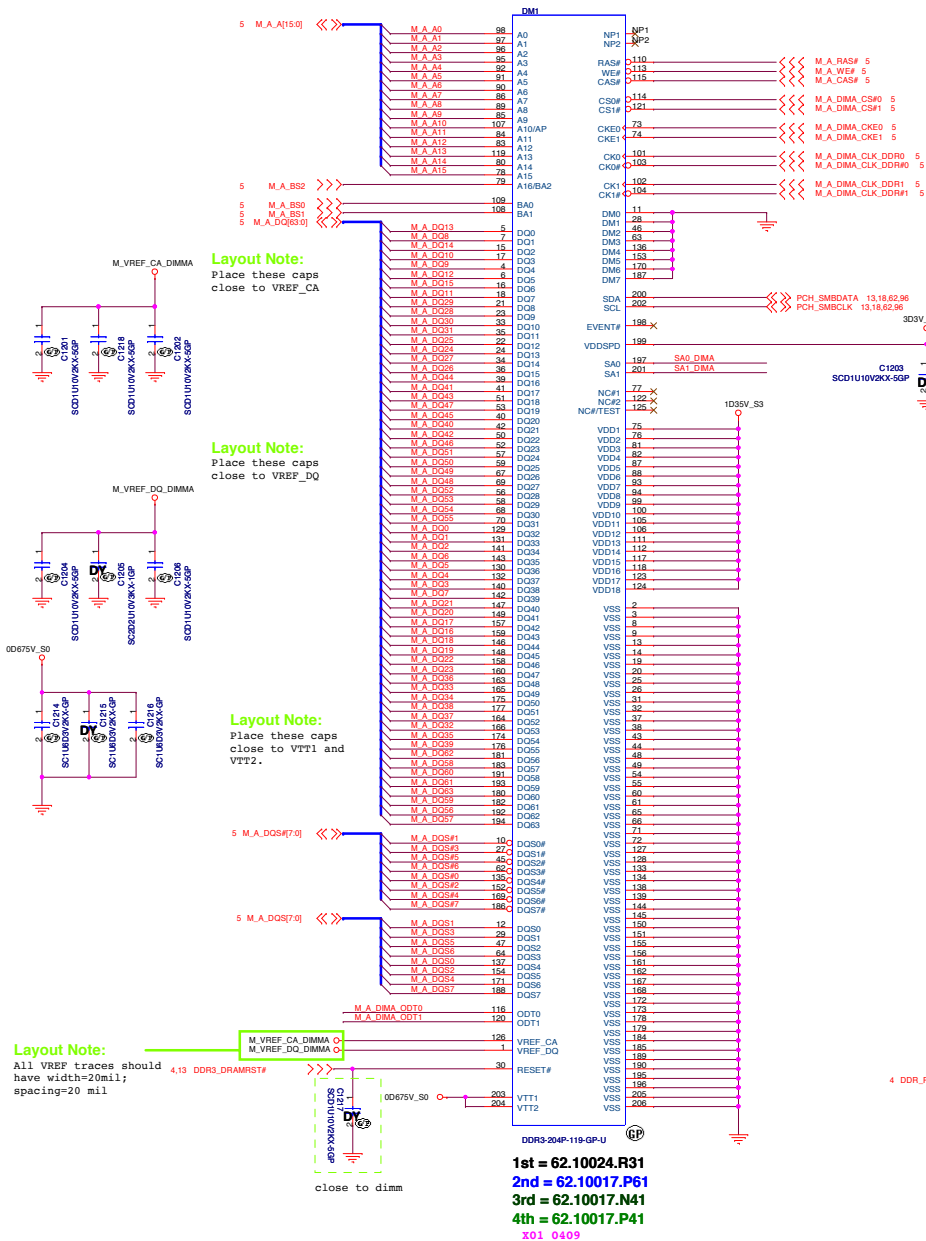
X00

Date: Wednesday, April 10, 2013

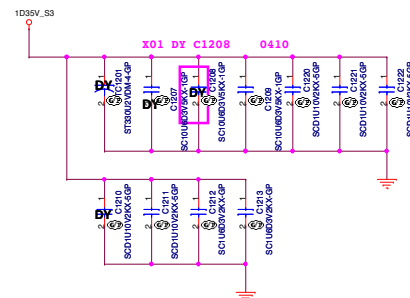
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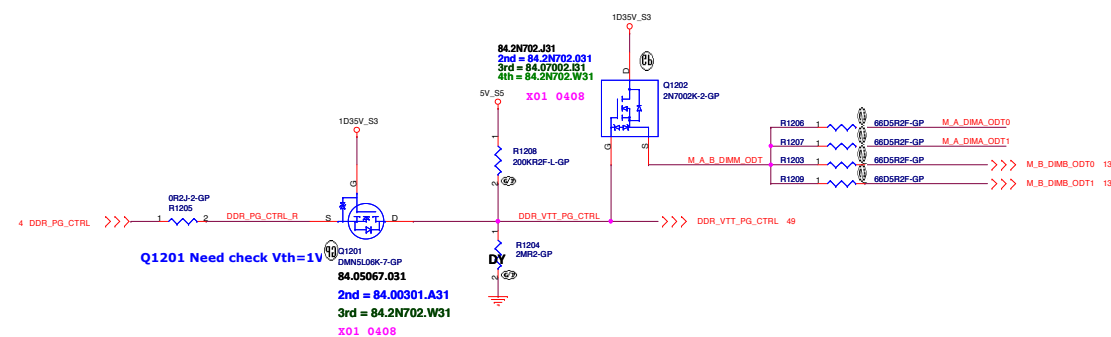
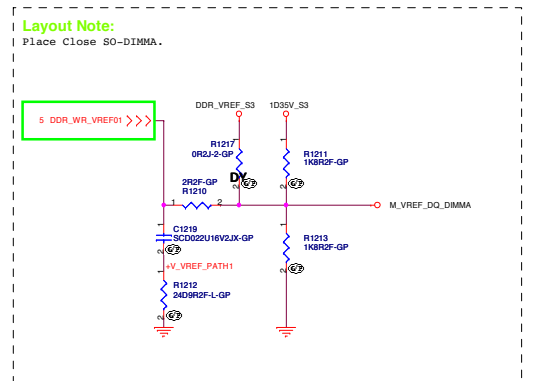
## SSID = MEMORY



**Note:**  
SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30



**Layout Note:**  
Place these Caps near SO-DIMM.

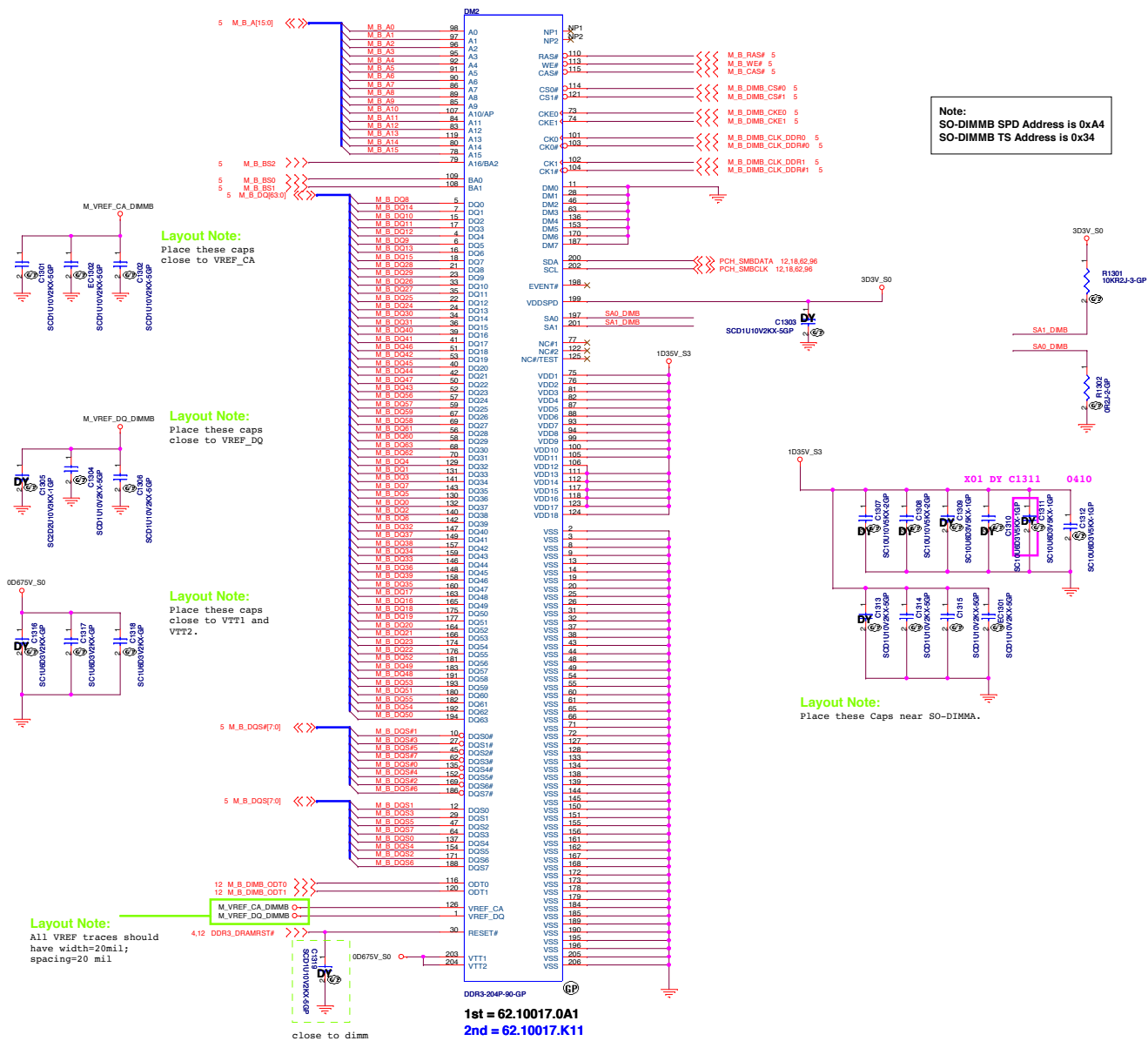


◀Core Design▶



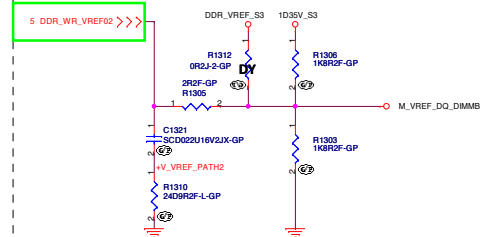
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|---------------------|----------------------------|-------------|-----|
| Title               |                            |             |     |
| <b>DDR3-SODIMM1</b> |                            |             |     |
| Size<br>A2          | Document Number            | Rev         |     |
|                     | <b>Latitude300 Haswell</b> | <b>X0</b>   |     |
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## SSID = MEMORY

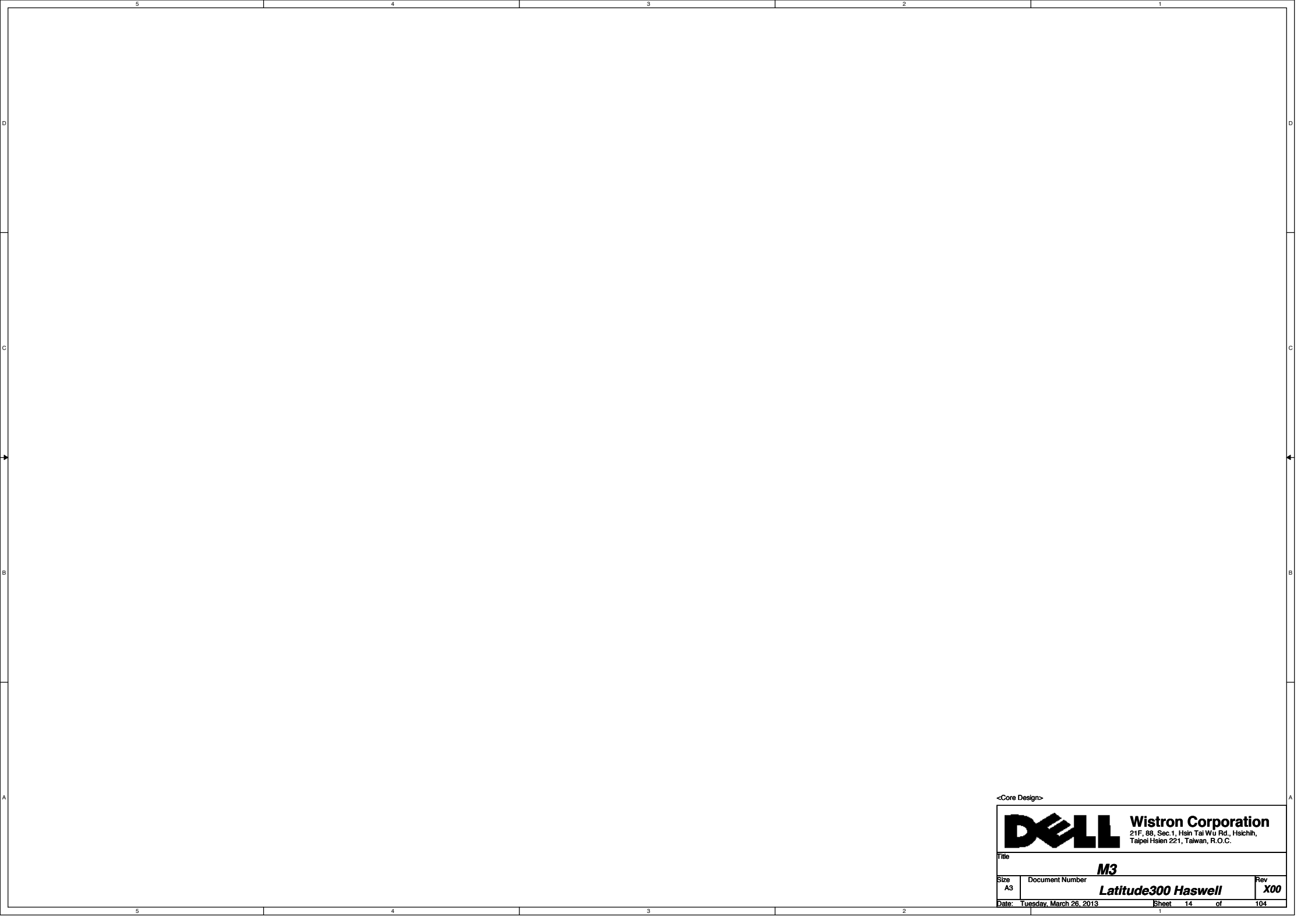


**Note:**  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34


**Layout Note:**  
Place Close SO-DIMMA.



1st = 62.10017.0A1  
2nd = 62.10017.K11  
3rd = 62.10017.P31  
4th = 62.10017.N91  
x01 0409



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|   |                            |  |            |
|---|----------------------------|--|------------|
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| Title   |                            |  |            |
| <b>M3</b>   |                            |  |            |
| Size  | Document Number            |  | Rev        |
| A3  | <b>Latitude300 Haswell</b> |  | <b>X00</b> |
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<Core Design>

|   |                        |  |           |
|---|------------------------|--|-----------|
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| Title   |                        |  |           |
|   |                        | <b><i>PCH ( EDP/GPIO/DDI )</i></b>   |           |
| Size<br>A3  | Document Number        | <b><i>Latitude300 Haswell</i></b>  |           |
| Date:   | Friday, April 19, 2013 | Sheet  | 15 of 104 |

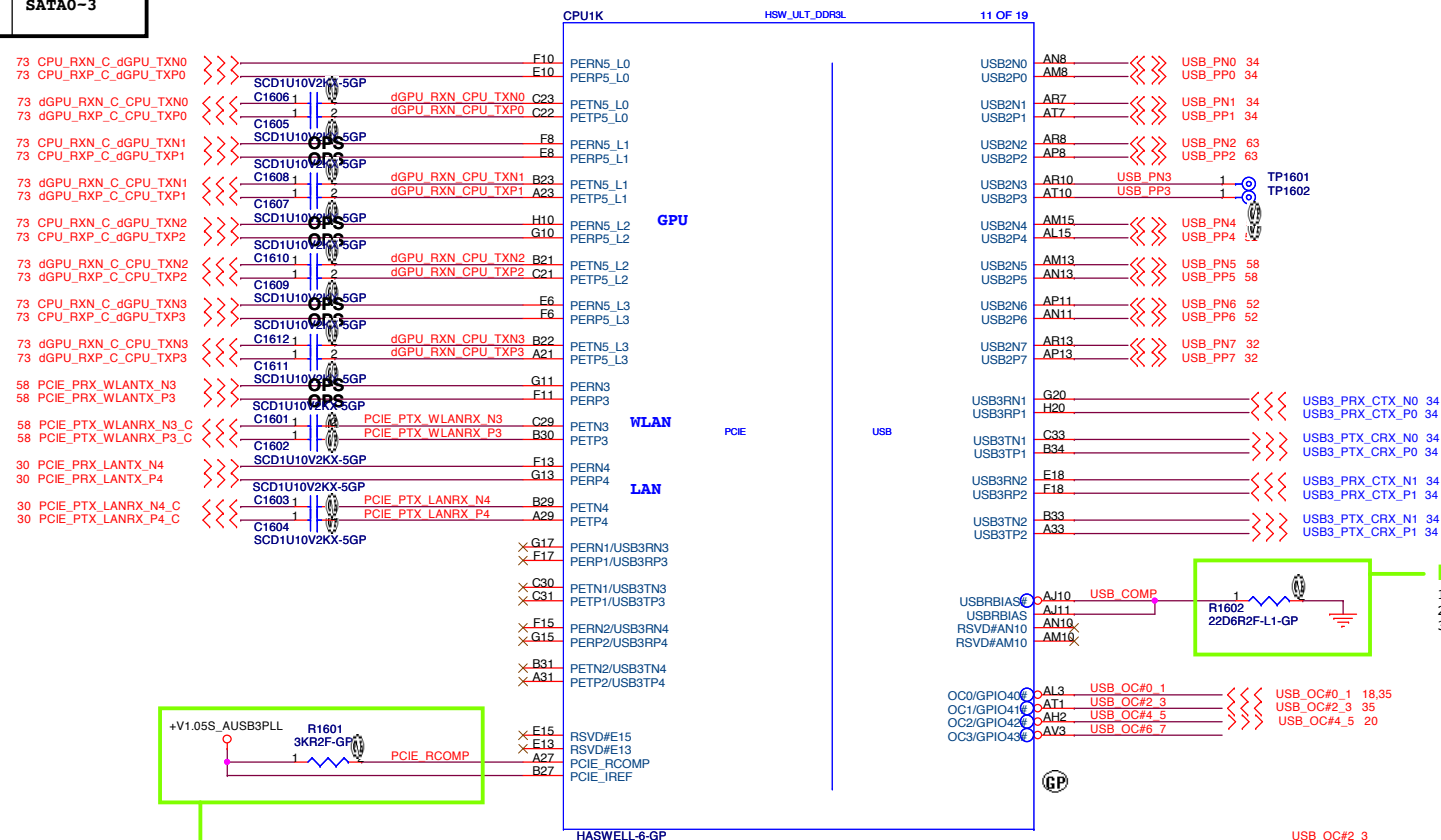
**SSID = PCH**

## PCIE Table

| Port     | Device | Share BUS |
|----------|--------|-----------|
| 1        | TBD    | USB3.0_3  |
| 2        | TBD    | USB3.0_4  |
| 3        | WLAN   |           |
| 4        | LAN    |           |
| 5(4lane) | GPU    |           |
| 6(4lane) | TBD    | SATA0-3   |

## USB 2.0 Table

| Pair | Device       |
|------|--------------|
| 0    | USB3.0 port1 |
| 1    | USB3.0 Port2 |
| 2    | USB2.0 Port3 |
| 3    | TBD          |
| 4    | CAMERA       |
| 5    | WLAN         |
| 6    | Touch Panel  |
| 7    | Card Reader  |



**Layout Note:**

1. PCIe\_RCOMP/ PCIe\_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

- **Layout Note:**

1. USB\_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil



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Title

### **PCH (PCIE/USB)**

Size  
A

|                 |
|-----------------|
| Document Number |
|-----------------|

**Latitude300 Haswell**

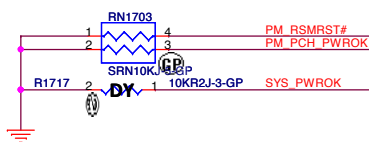
|     |     |
|-----|-----|
| Rev | X00 |
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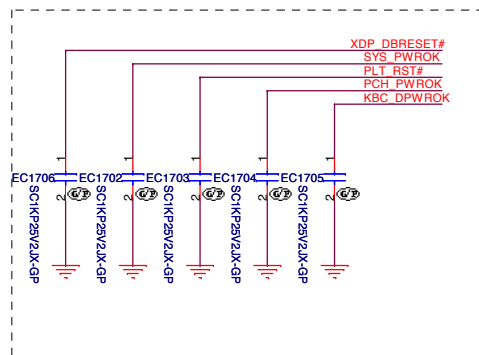
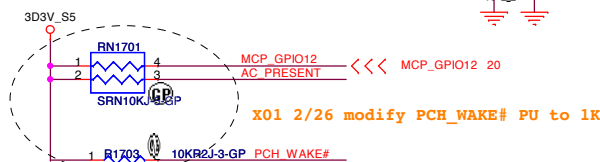
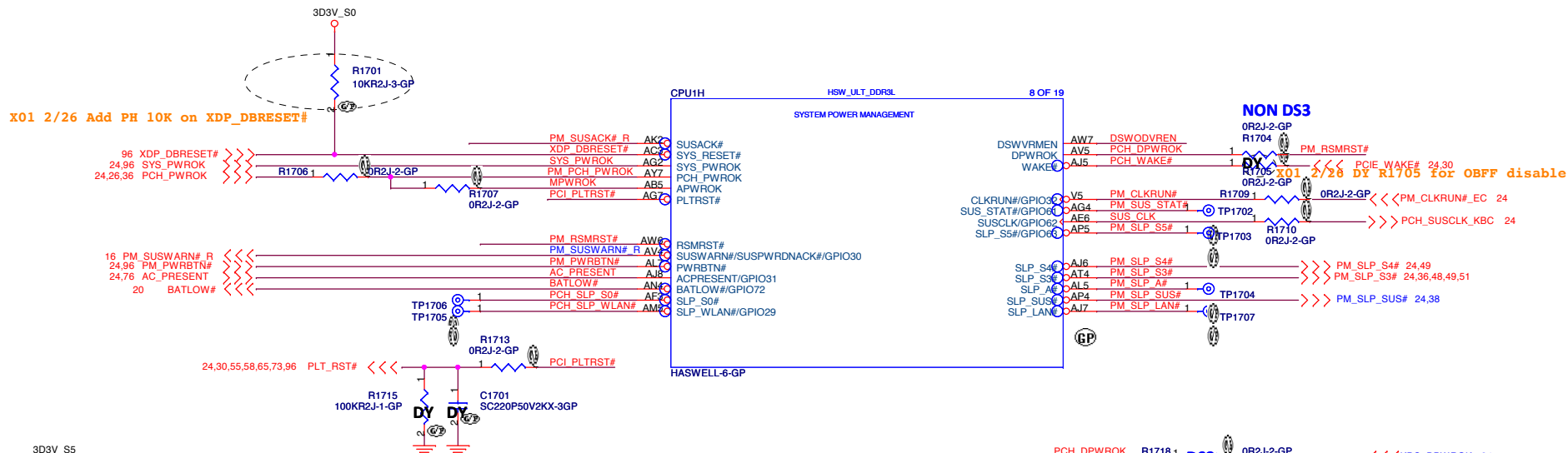
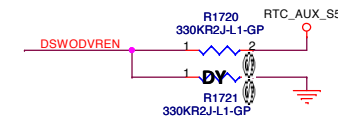


## SSID = PCH

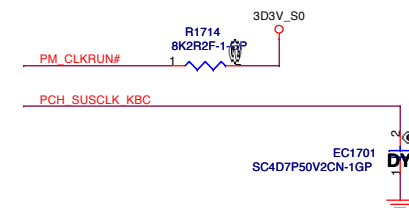
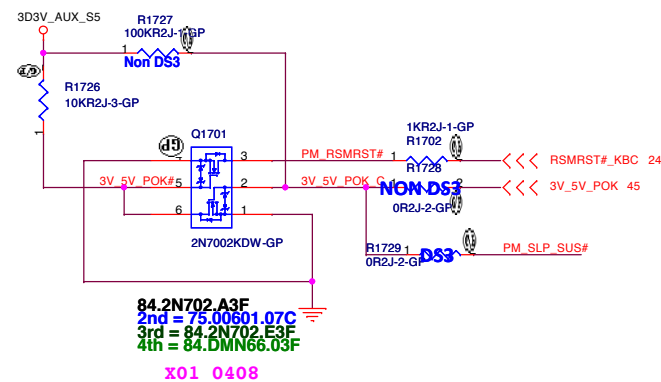
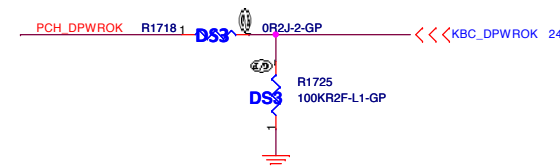
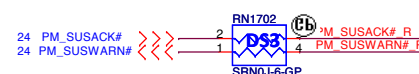


**PCH strap pin:**

| On Die DSW VR Enable |  |
|----------------------|--|
| DSWODVREN            | Low = Disable<br>* High = Enable (default) |



EMI 12/20



## <Core Design>

DELL

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| Title | Author | Date | Page |
|-------|--------|------|------|
| Title | Author | Date | Page |

**PCH (PM)**

Size

|                 |
|-----------------|
| Document Number |
|-----------------|

**Latitude300 Haswell**

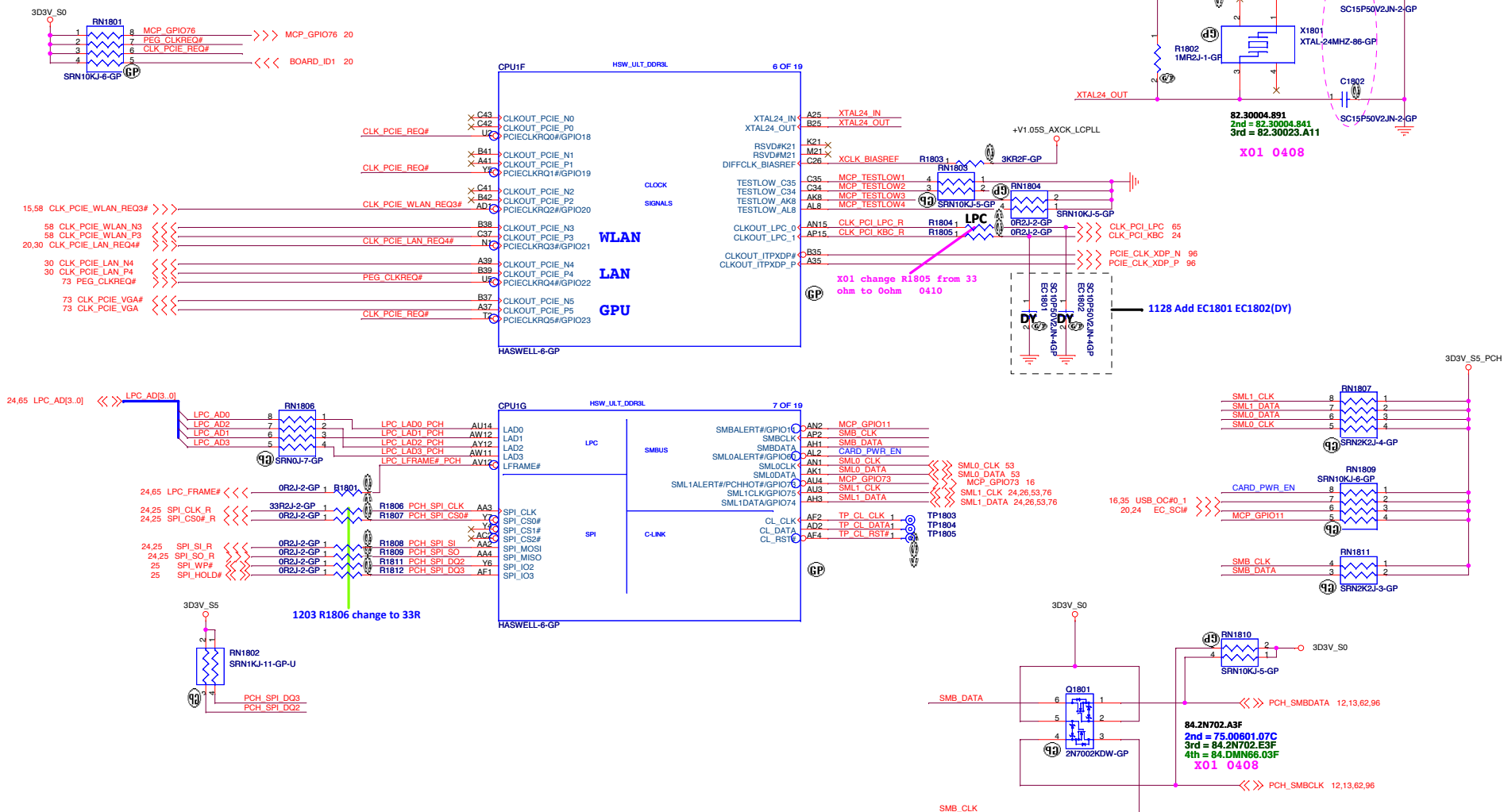
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**SSID = PCH**

X01 Follow vendor's suggestion,  
change C1801 C1802 to 15p 0417



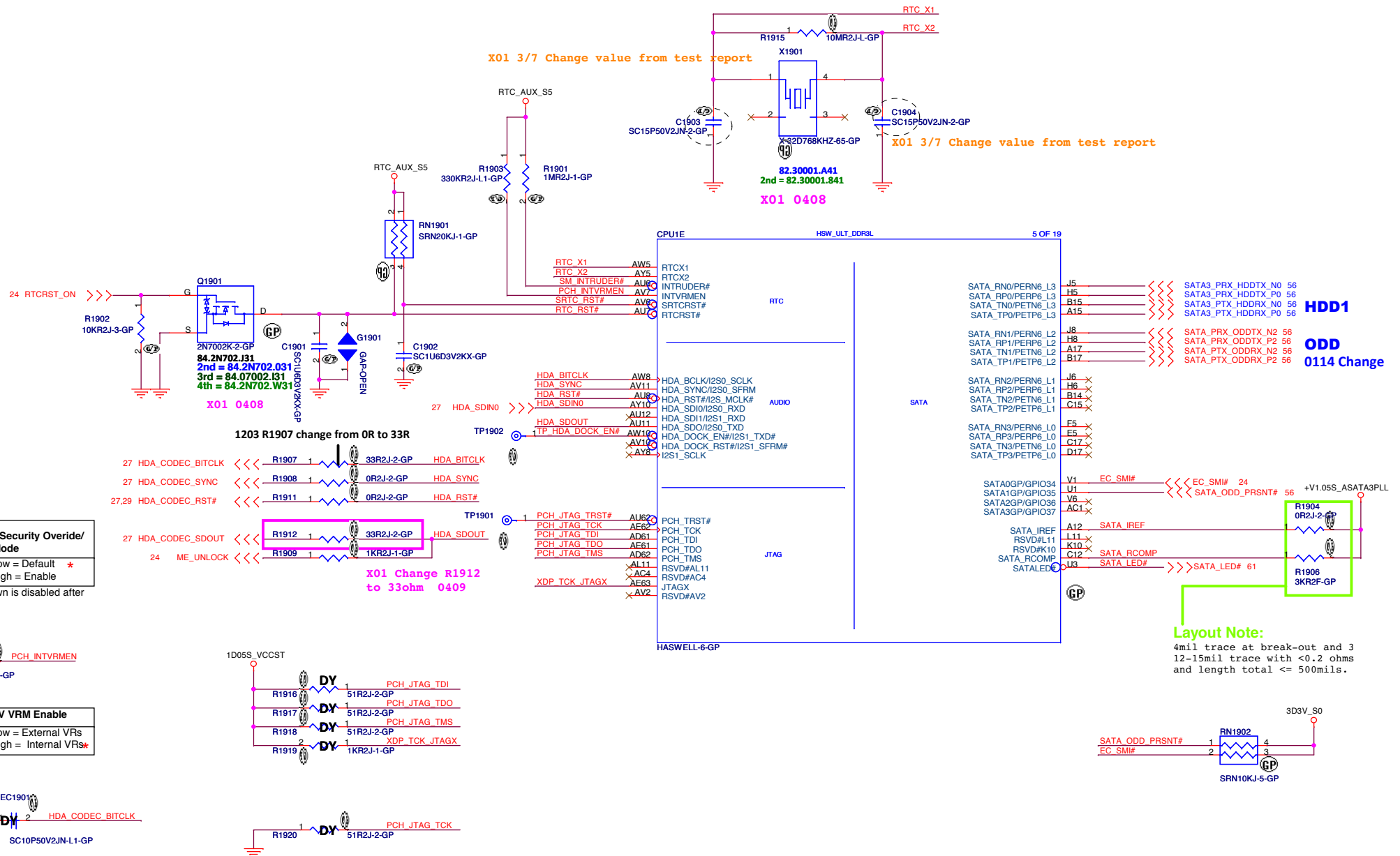
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|                                     |                            |             |     |
|-------------------------------------|----------------------------|-------------|-----|
| Title                               |                            |             |     |
| <b>PCH (CLOCK/SMBUS/CL/LPC/SPI)</b> |                            |             |     |
| Size                                | Document Number            | Rev         |     |
| Custom                              | <b>Latitude300 Haswell</b> | Xv          |     |
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**SSID = CPU**



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Title

### **PCH (RTC/SATA/HDA/JTAG)**

Size  
A

Document Number

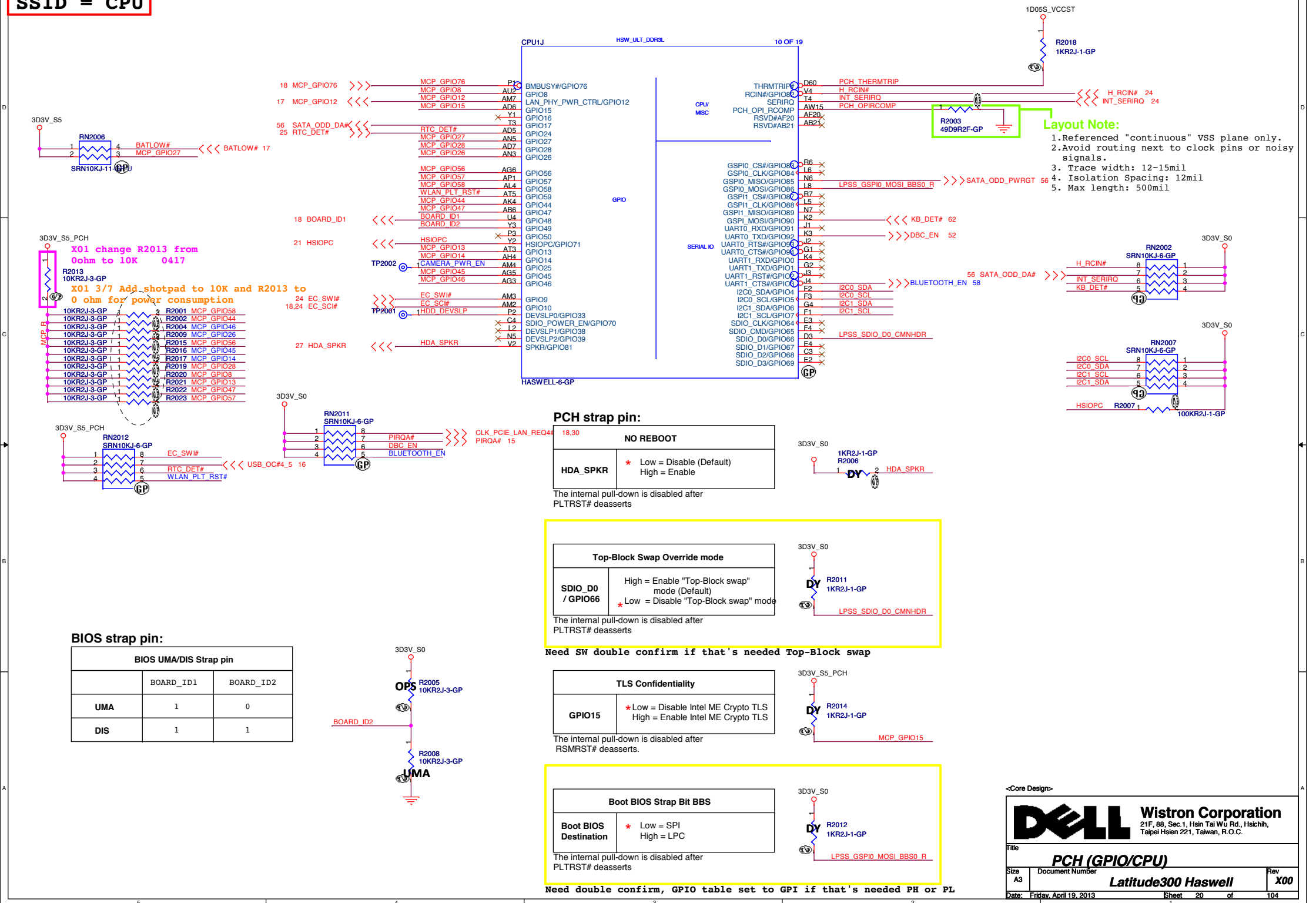
**Latitude300 Haswell**

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|-----|-----|
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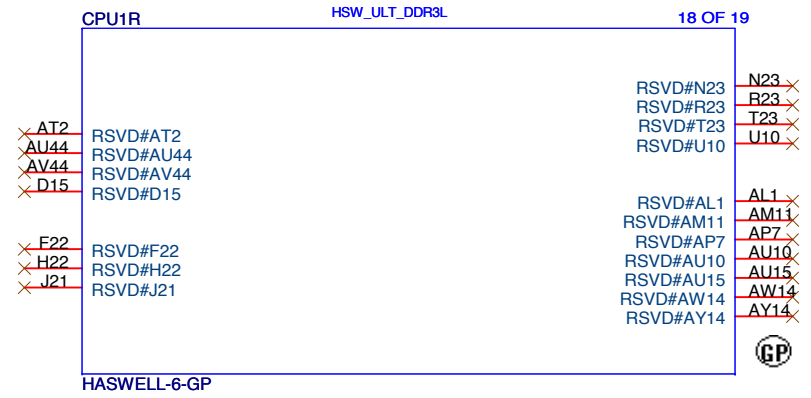
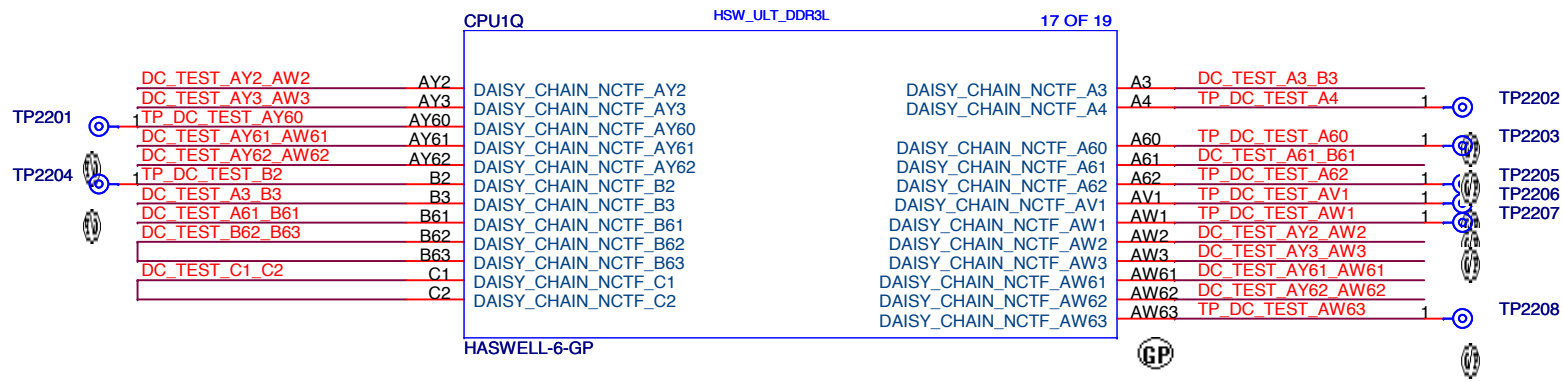
**SSID = CPU**



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|---|--|--|--|
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| Title   |  |  |  |
| Size A3   |  | <b>CPU (POWER2)</b><br><b>Latitude300 Haswell</b>  |  |
| Document Number   |  | Rev  |  |
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|   |  | <b>X00</b>   |  |

SSID = PCH



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Title

(Reserved)

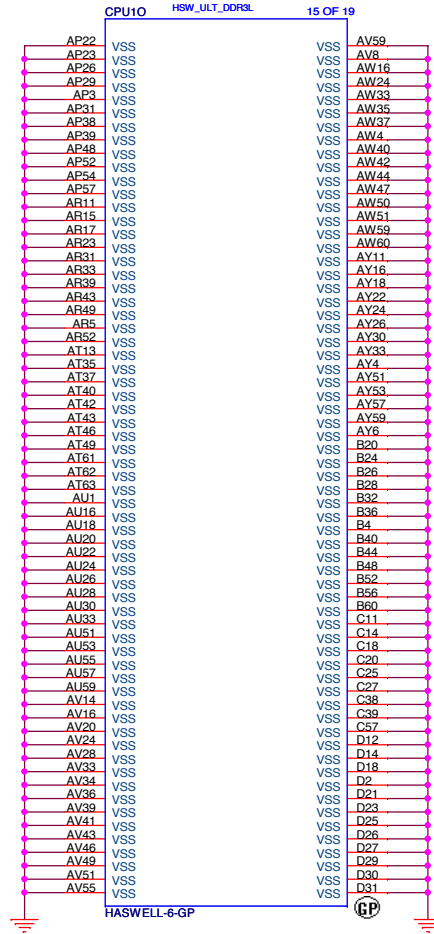
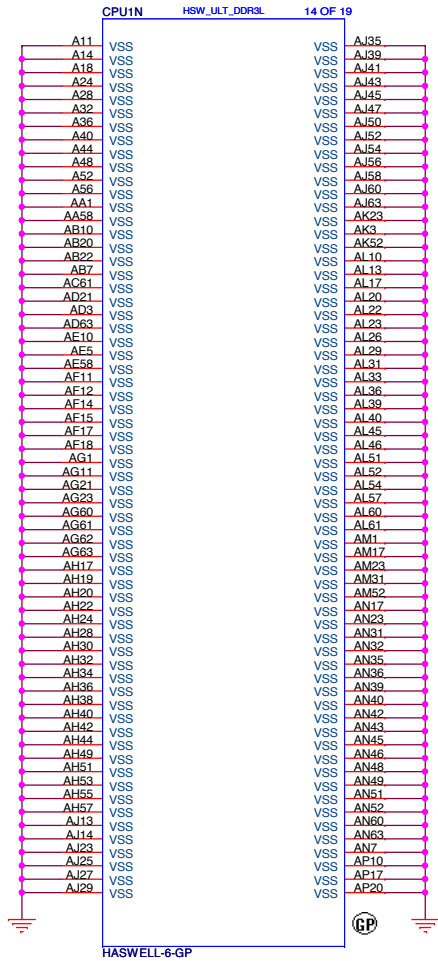
SizeA4

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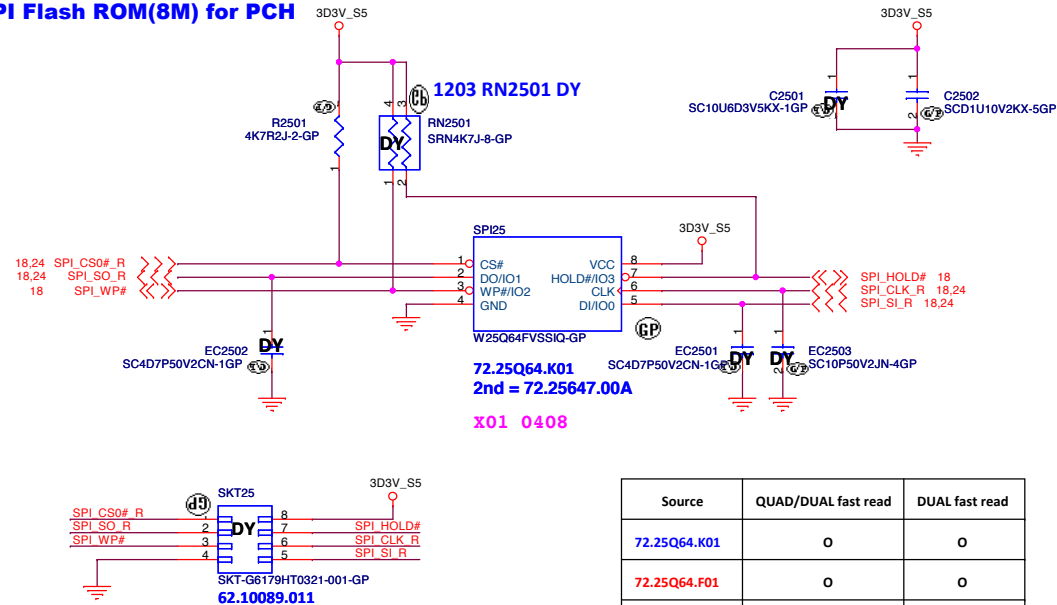
SSID = PCH





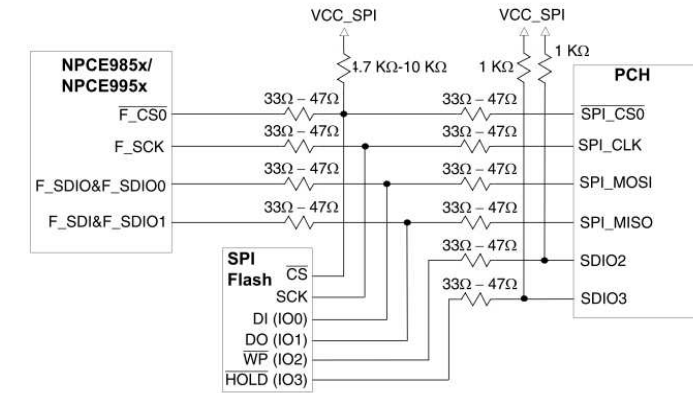


### SPI Flash ROM(8M) for PCH



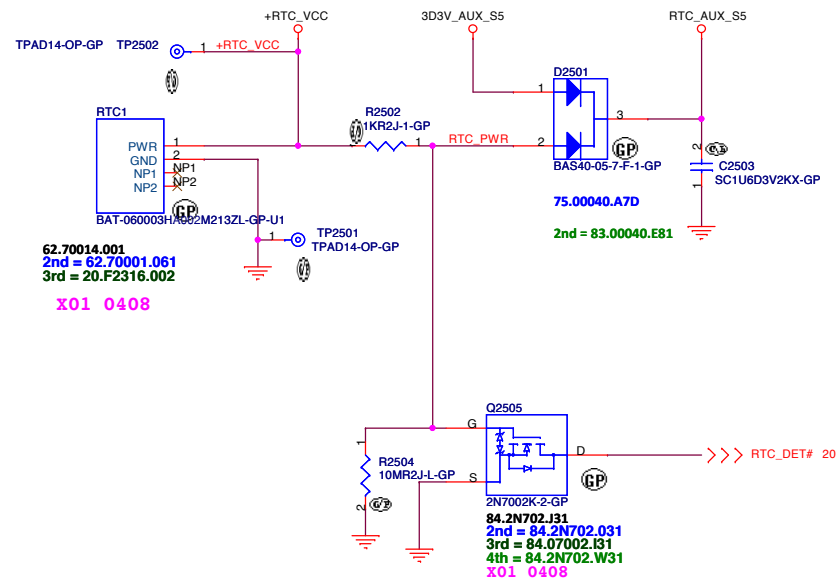
| Source       | QUAD/DUAL fast read | DUAL fast read |
|--------------|---------------------|----------------|
| 72.25Q64.K01 | 0                   | 0              |
| 72.25Q64.F01 | 0                   | 0              |
| 72.25Q64.D01 | 0                   | 0              |

### Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

**SSID = RBATT**



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| Title | Author | Year | Journal | Volume | Page |
|-------|--------|------|---------|--------|------|
| ...   | ...    | ...  | ...     | ...    | ...  |

Flash/RTC

Size  
A2

| Document Number |
|-----------------|
|-----------------|

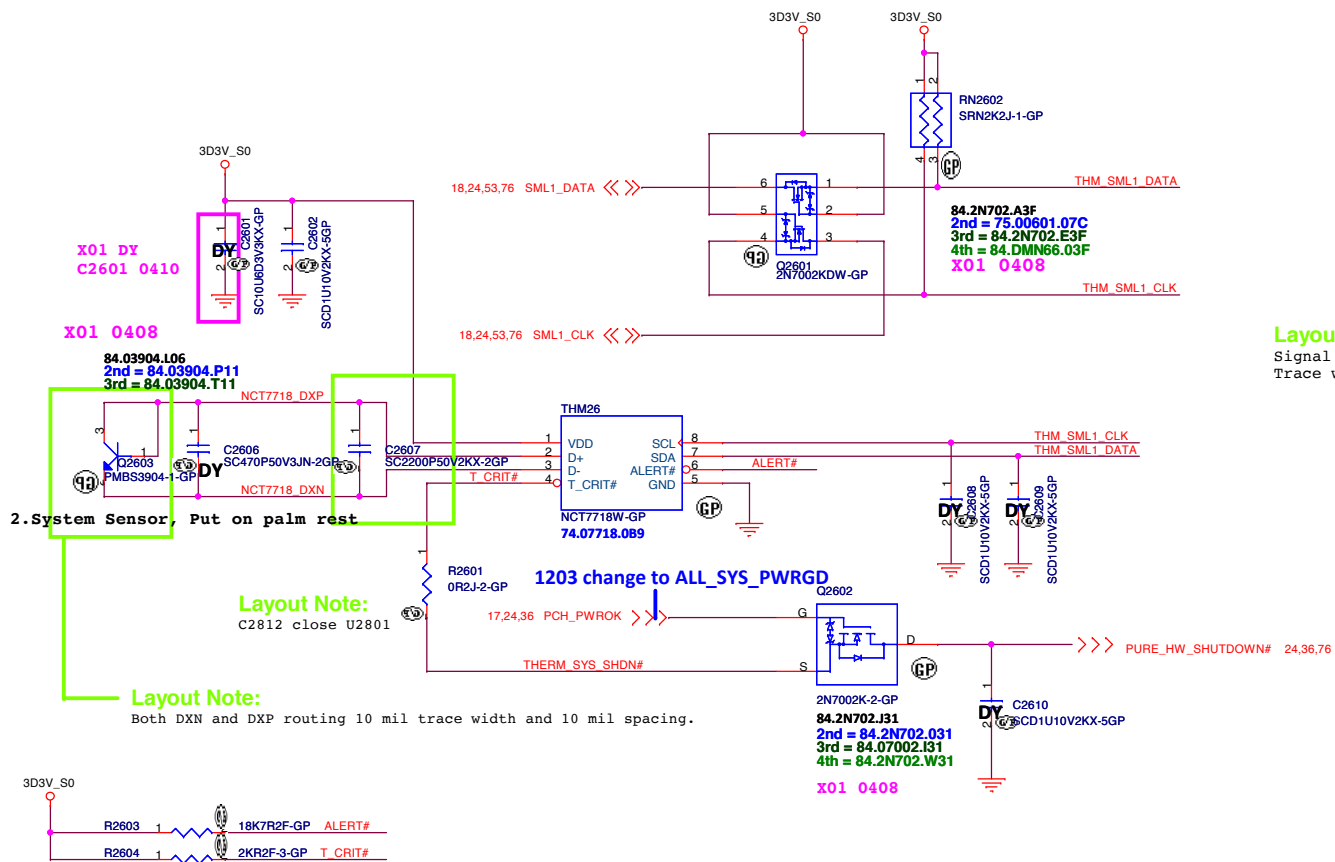
**Latitude300 Haswell**

Rev  
K22

Date: Friday, April 19, 2013

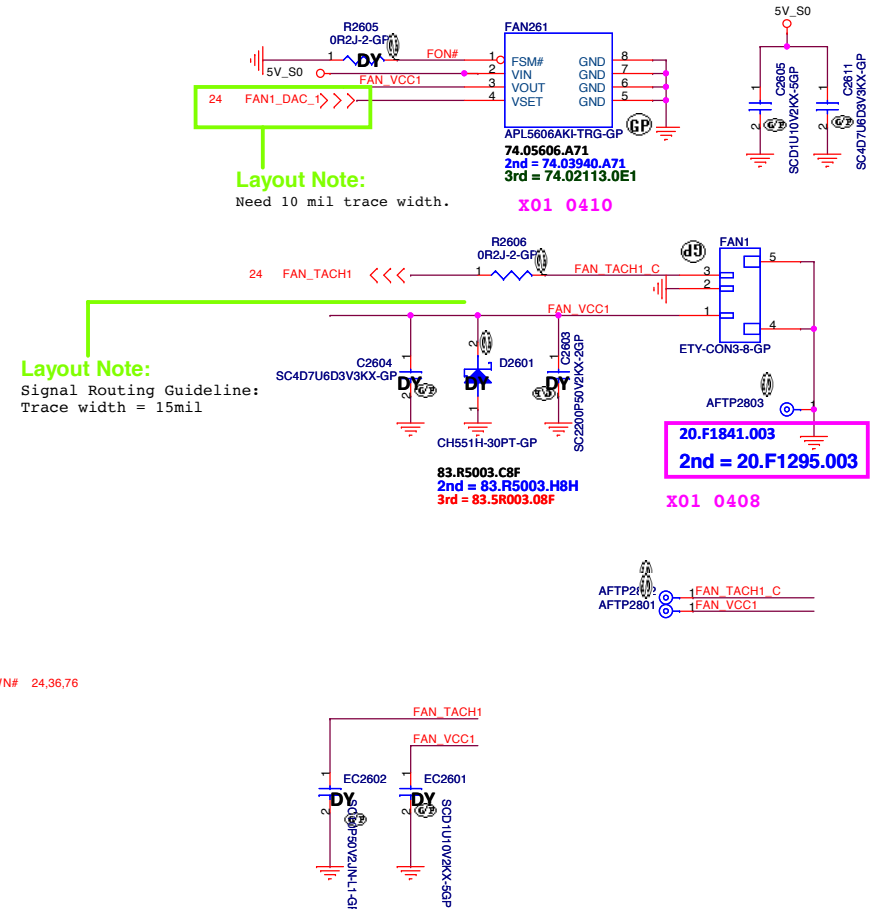
Sheet 25 of 104

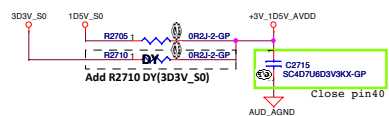
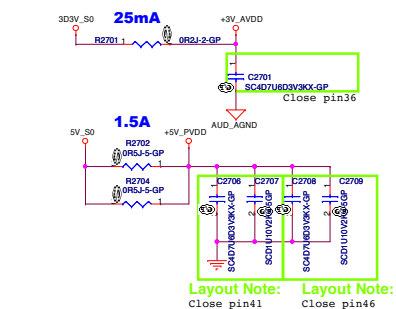
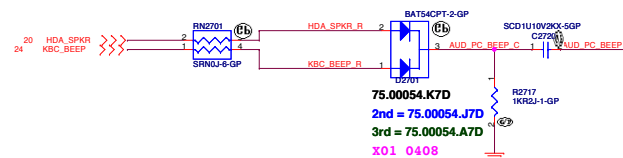
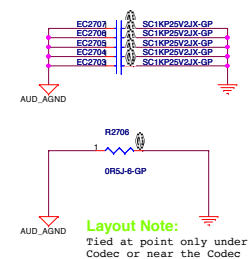
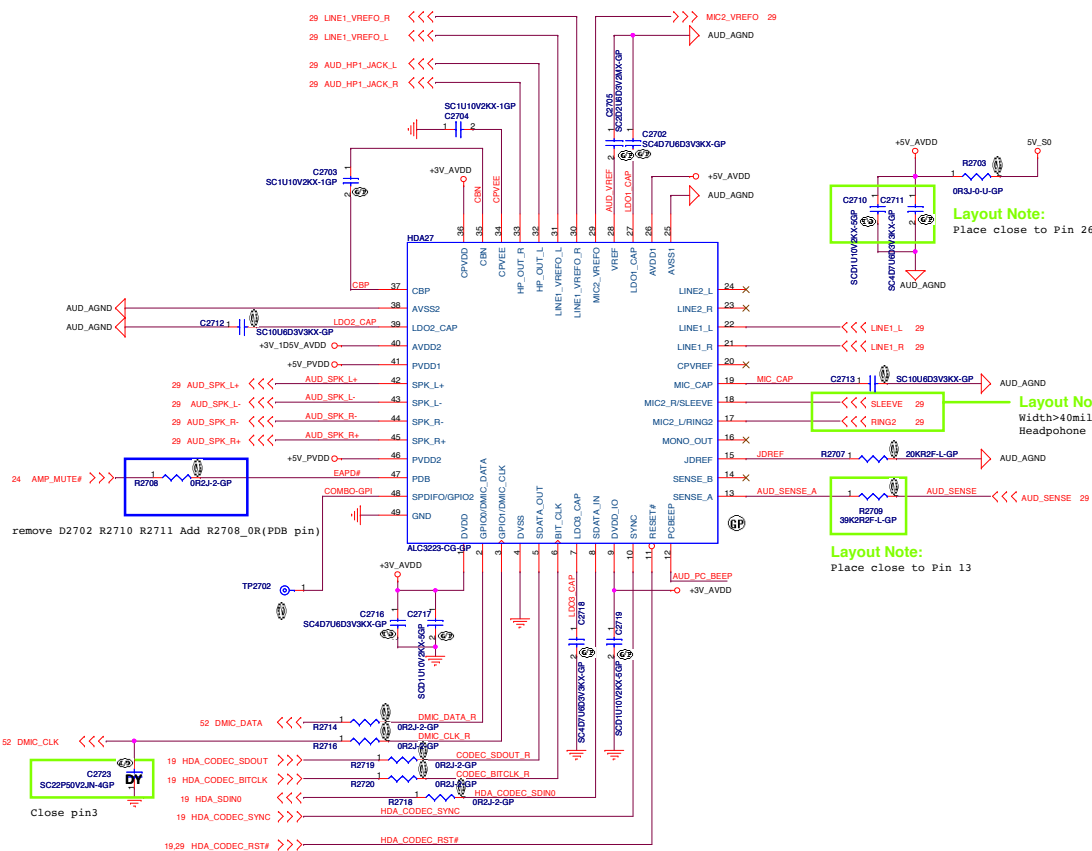
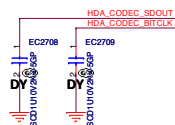
**SSID = Thermal**



| TEMPERATURE (°C) |        | T_CRIT# |       |        |      |        |
|------------------|--------|---------|-------|--------|------|--------|
|                  |        | 2KΩ     | 7.5KΩ | 10.5KΩ | 14KΩ | 18.7KΩ |
| ALERT#           | 2KΩ    | 77      | 87    | 97     | 107  | 117    |
|                  | 7.5KΩ  | 79      | 89    | 99     | 109  | 119    |
|                  | 10.5KΩ | 81      | 91    | 101    | 111  | 121    |
|                  | 14KΩ   | 83      | 93    | 103    | 113  | 123    |
|                  | 18.7KΩ | 85      | 95    | 105    | 115  | 125    |


## Fan controller1



**SSID = AUDIO****Azalia I/F EMI**

(Blanking)

<Core Design>



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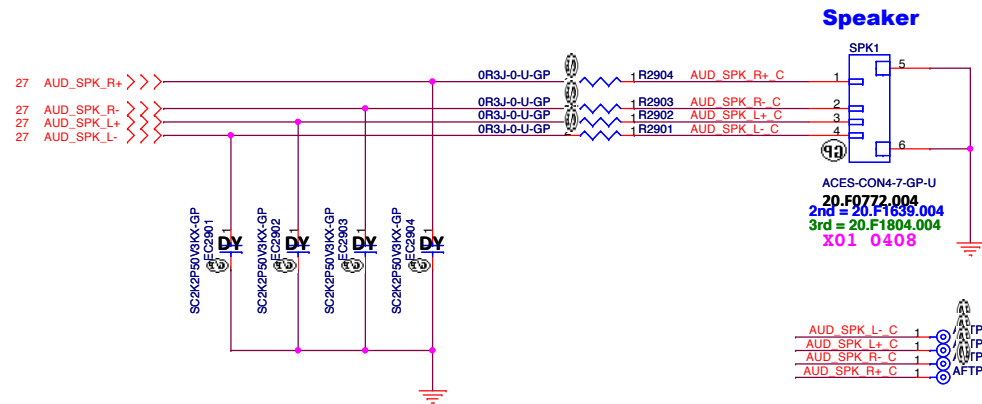
Title

**Reserved**

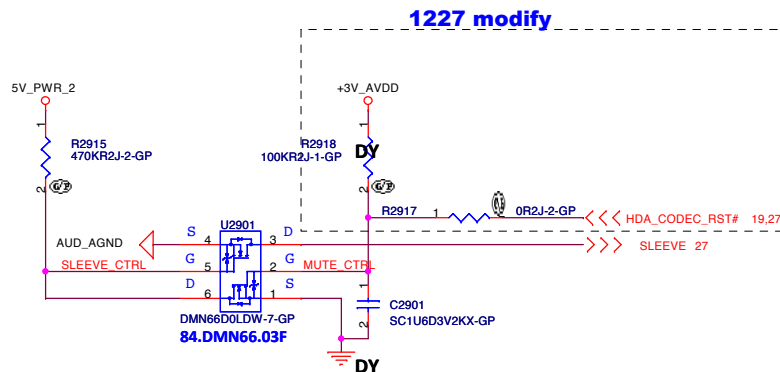
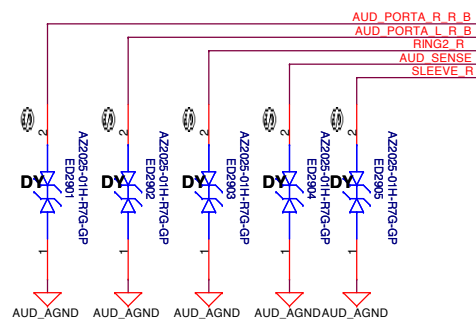
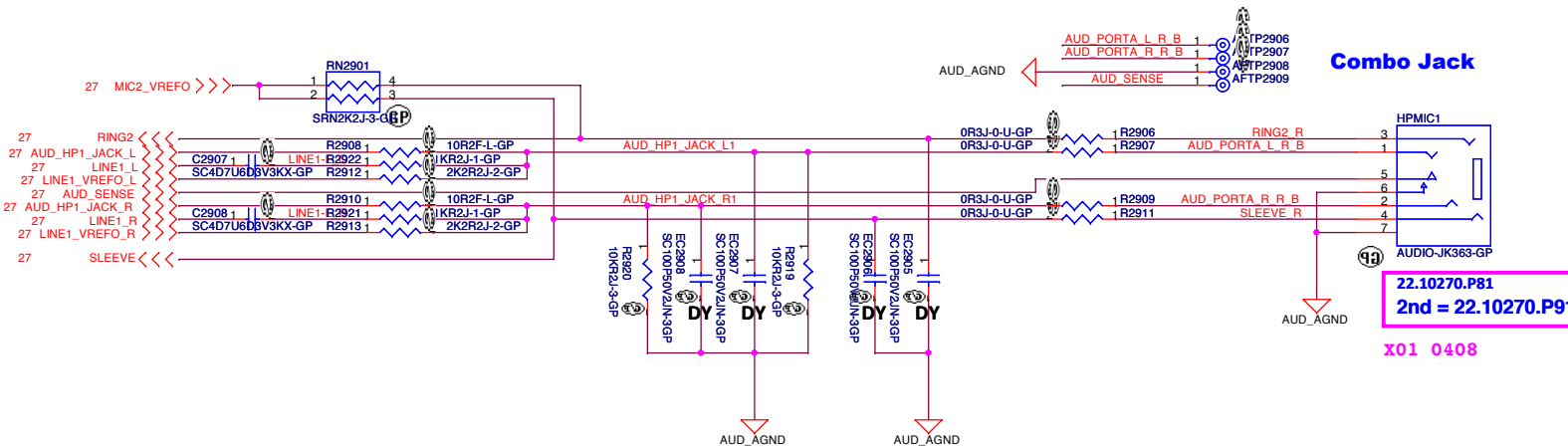
|      |                            |            |
|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                 |
|-------------------------------|-----------------|
| Date: Tuesday, March 26, 2013 | Sheet 28 of 104 |
|-------------------------------|-----------------|

# SSID = AUDIO

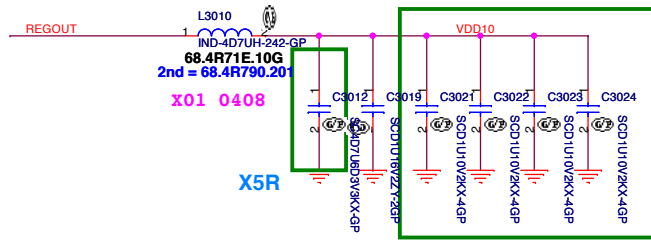


| CONN Pin | Net name |
|----------|----------|
| Pin1     | SPK_R+   |
| Pin2     | SPK_R-   |
| Pin3     | SPK_L+   |
| Pin4     | SPK_L-   |

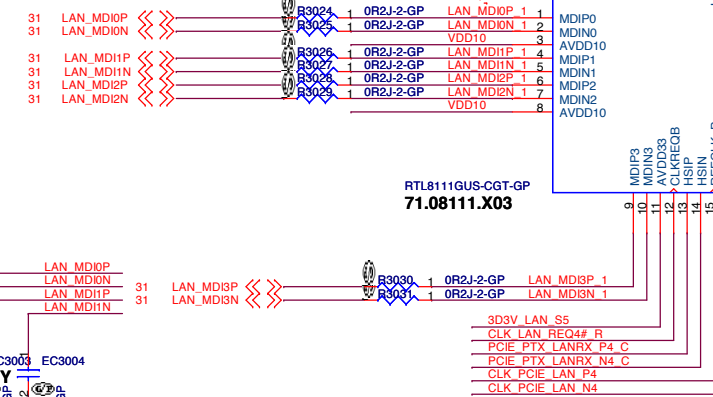
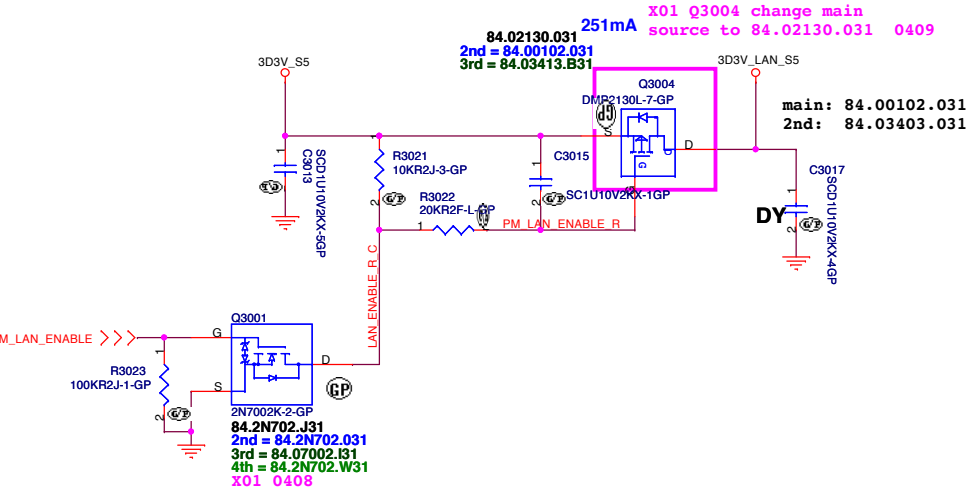
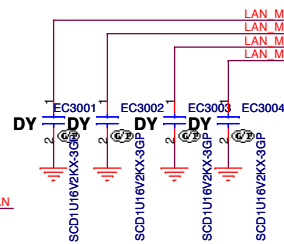
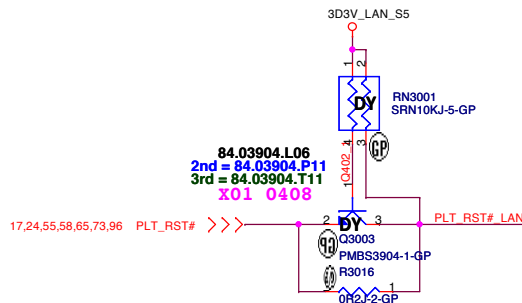
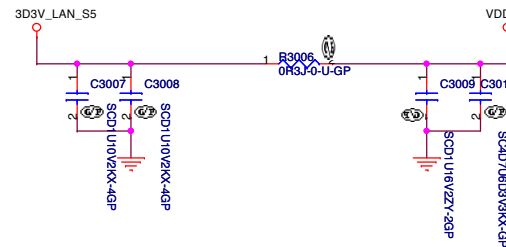


# LAN CHIP

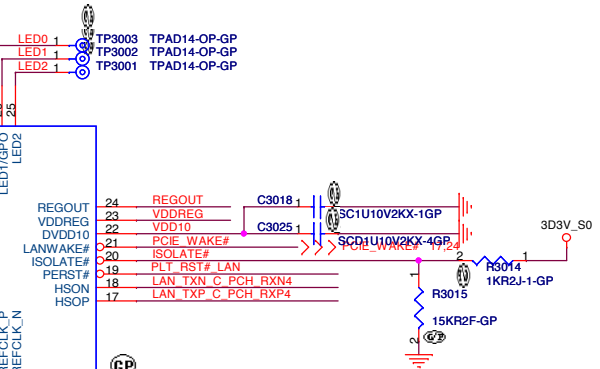
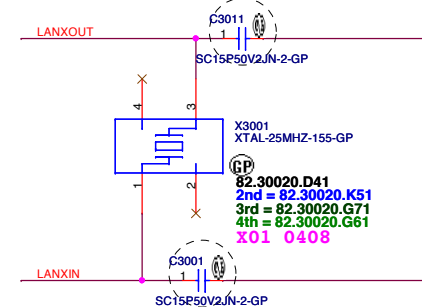
10/100 Need Only need C3021, C3022, C3023, C3024 in Pin3, 8, 22, 30



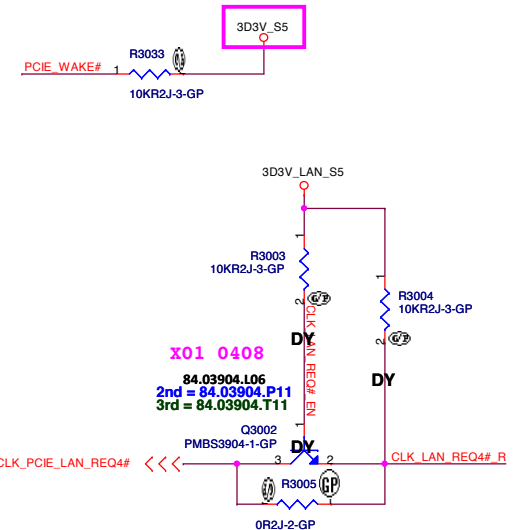
40 mils



**X00 3/7 Change value from test report**



```
X01 0405 change PCIE_WAKE#
power to 3D3V_S5
```



### <Core Design>

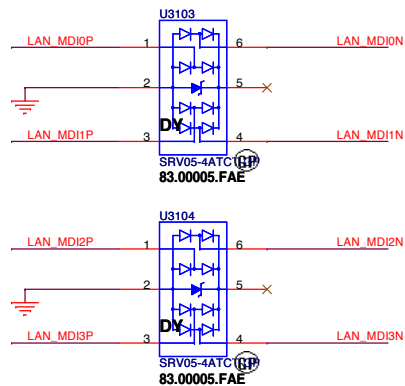
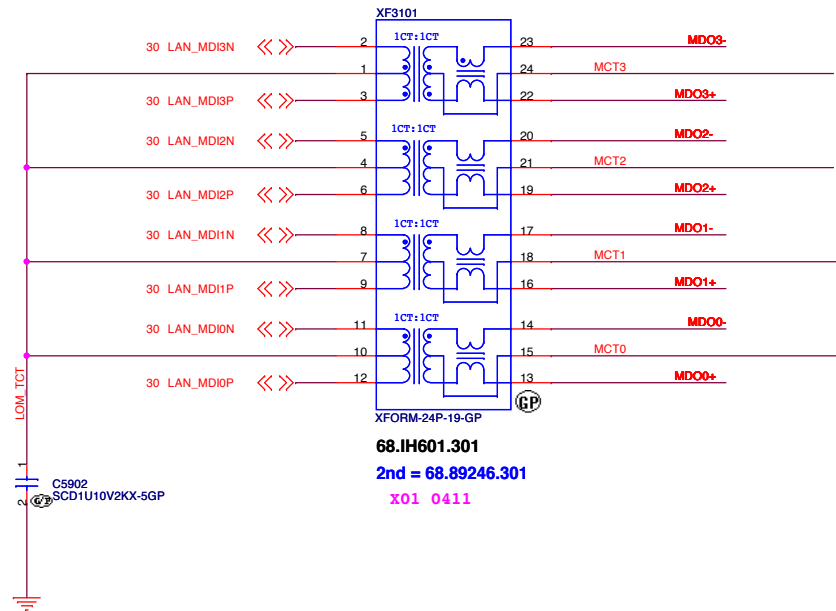


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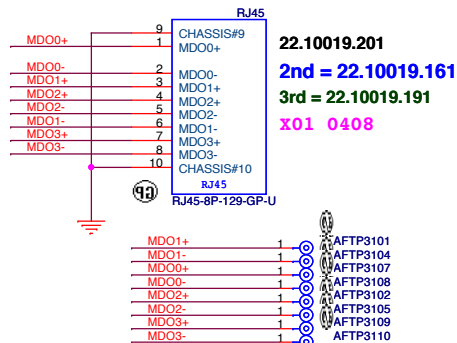
|            |                            |             |            |
|------------|----------------------------|-------------|------------|
| Title      |                            |             |            |
| <b>LOM</b> |                            |             |            |
| Size<br>A3 | Document Number            |             | Rev        |
|            | <b>Latitude300 Haswell</b> |             | <b>X00</b> |
| Date:      | Friday, April 19, 2013     | Sheet 30 of | 104        |

SSID = LOM

# 100/GIGA LAN TransFormer



## RJ45 CONN

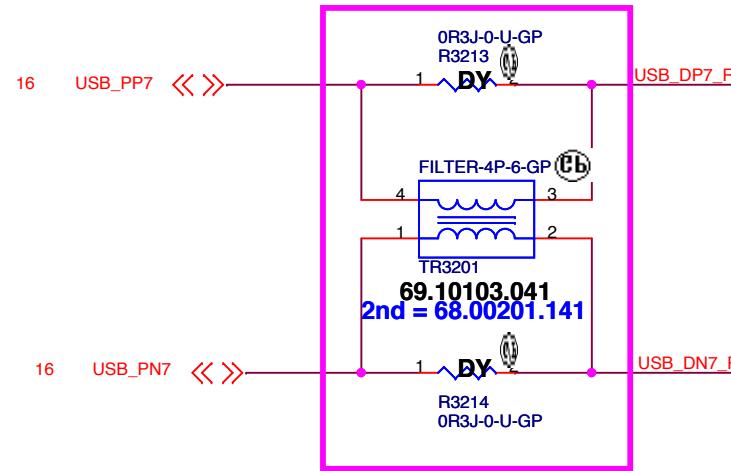
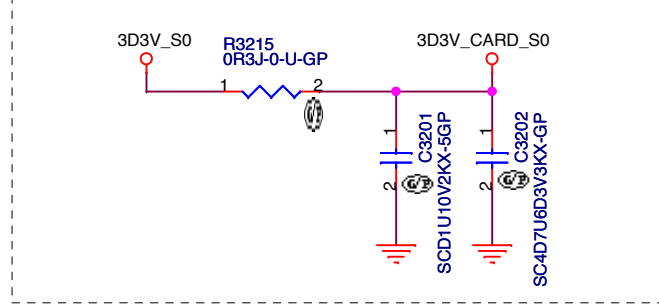


<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

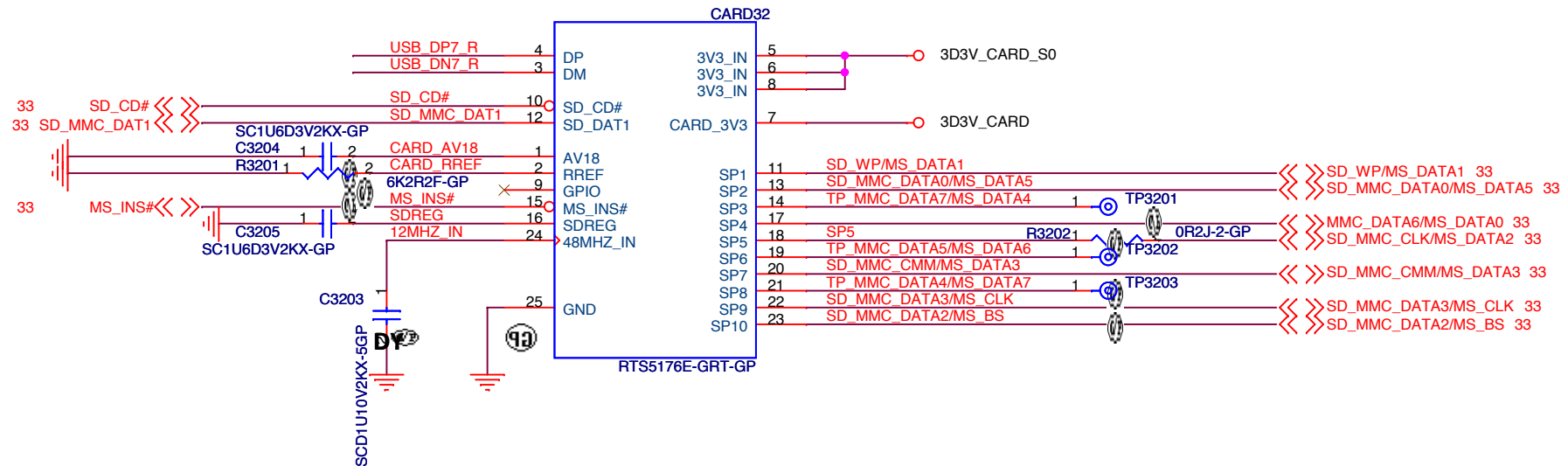
|       |                        |       |           |    |     |
|-------|------------------------|-------|-----------|----|-----|
| Title |                        |       | XFOM&RJ45 |    |     |
| Size  | Document Number        | Rev   |           |    |     |
| A3    | Latitude300 Haswell    | X00   |           |    |     |
| Date: | Friday, April 19, 2013 | Sheet | 31        | of | 104 |

# 1121 remove Switch(No support D3 cold)



X01 stuff TR3201,DY  
R3213,R3214 0415

| Pin name | Net name                |
|----------|-------------------------|
| SD_DAT1  | SD_MMC_DAT1             |
| SP1      | SD_WP/MS_DATA1          |
| SP2      | SD_MMC_DATA0/MS_DATA5   |
| SP3      | MMC_DATA7/MS_DATA4      |
| SP4      | MMC_DATA6/MS_DATA0      |
| SP5      | SD_MMC_CLK/MS_DATA2     |
| SP6      | MMC_DATA5/MS_DATA6      |
| SP7      | SD_MMC Command/MS_DATA3 |
| SP8      | MMC_DATA4/MS_DATA7      |
| SP9      | SD_MMC_DATA3/MS_CLK     |
| SP10     | SD_MMC_DATA2/MS_BS      |



<Core Design>



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Title

**Card Reader-RTS5176**

Size  
A4

Document Number

**Latitude300 Haswell**

Rev

**X00**

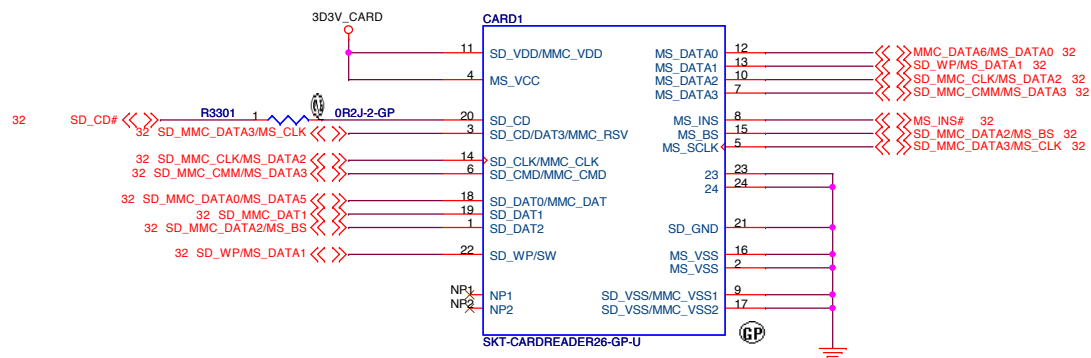
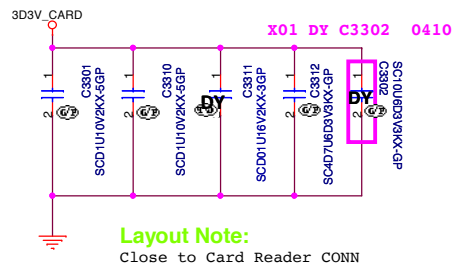
Date: Friday, April 19, 2013

Sheet 32 of 104

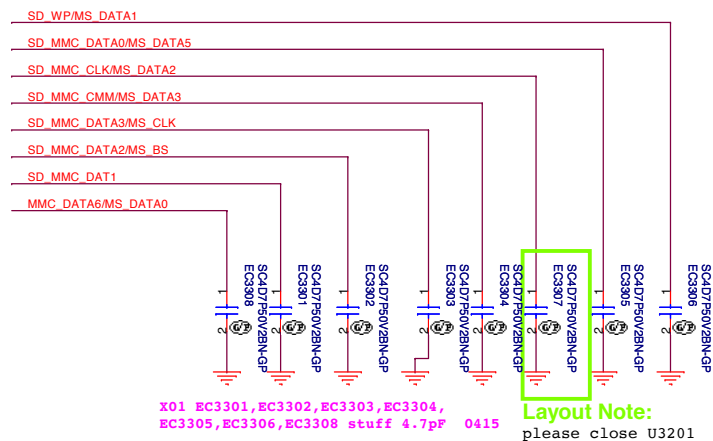


SSID = SDIO

## SD/MS/MMC Card Connector



## For EMI Reserved



1203 modify 10P change to 4.7P

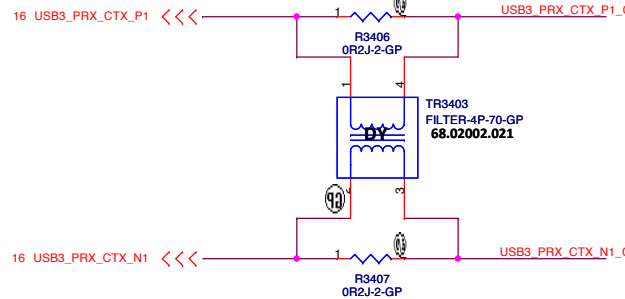
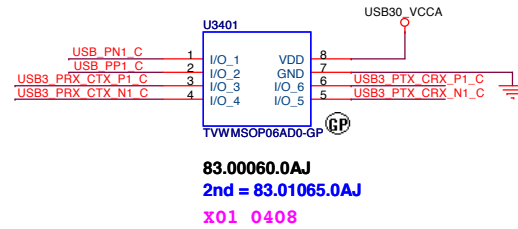
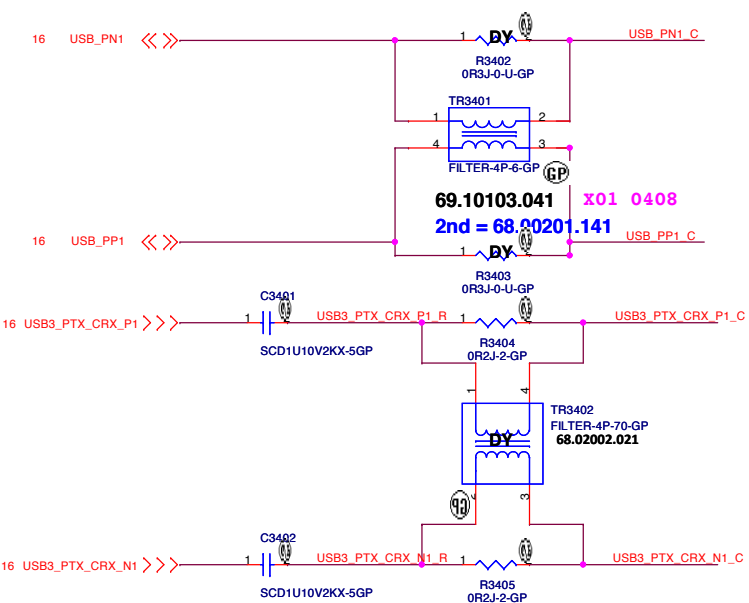
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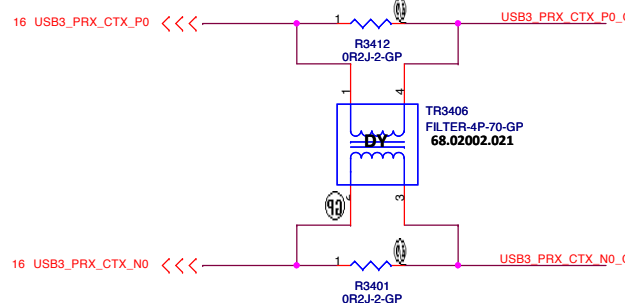
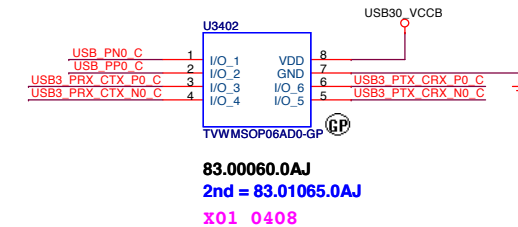
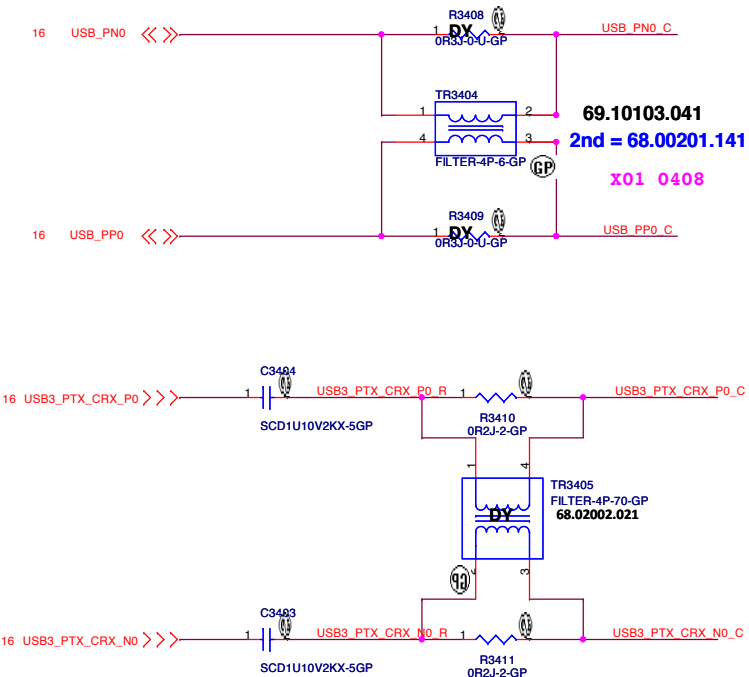
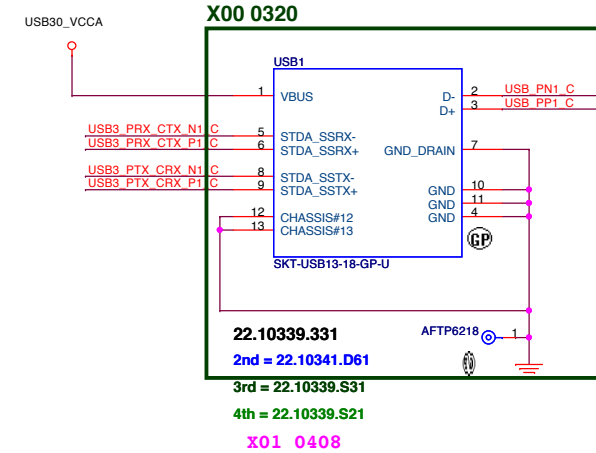
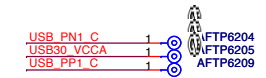
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|       |                        |       |                        |        |
|-------|------------------------|-------|------------------------|--------|
| Title |                        |       | SD/XD/MS/MMC Card CONN |        |
| Size  | Document Number        |       | Rev                    |        |
| A3    | Latitude300 Haswell    |       | X00                    |        |
| Date: | Friday, April 19, 2013 | Sheet | 33                     | of 104 |

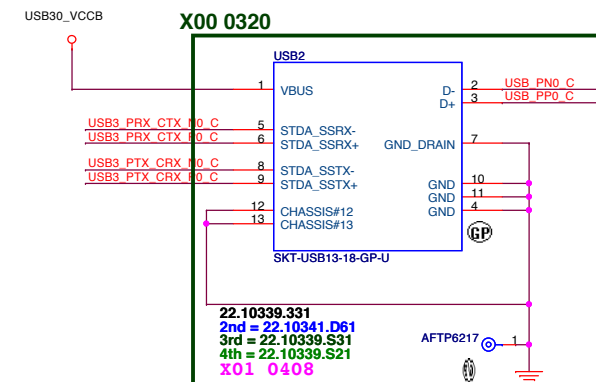
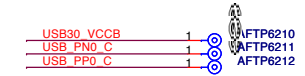
# SSID = USB



## USB3.0 Port1



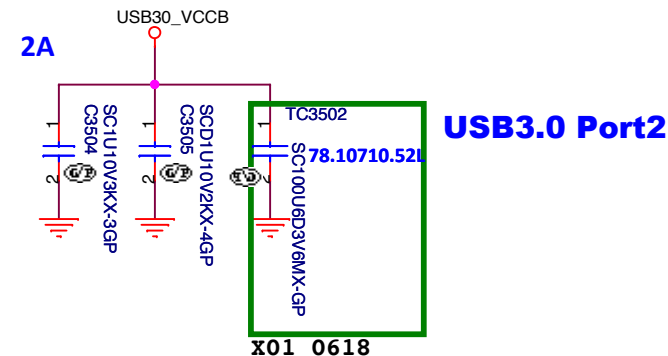
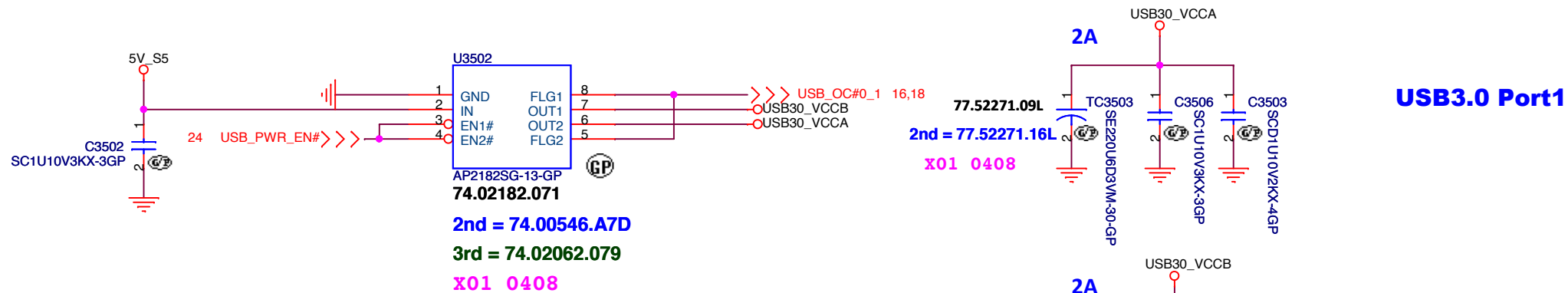
## USB3.0 Port2



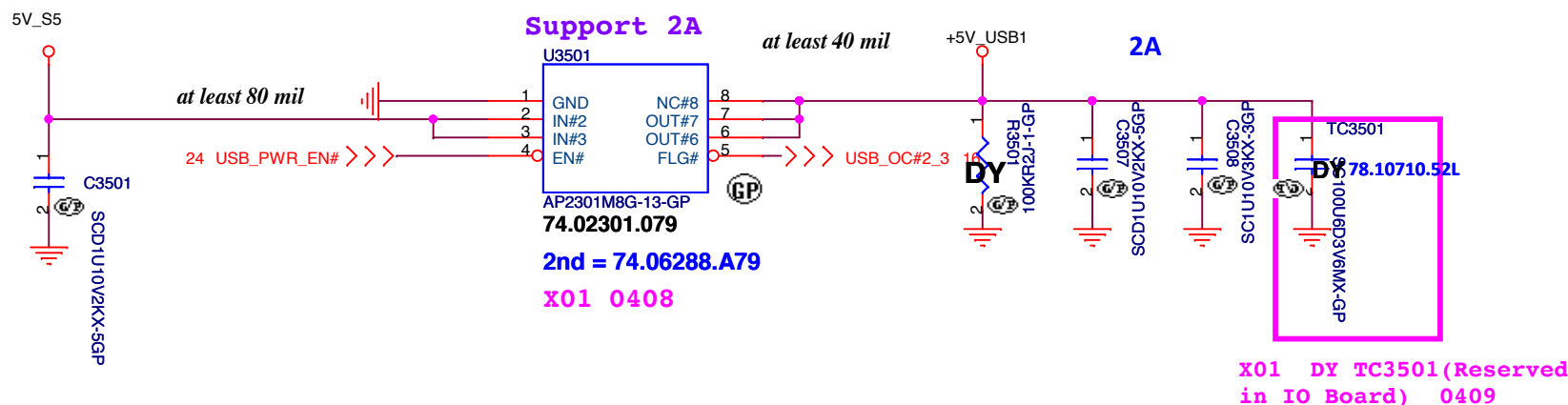
<Core Design>



|       |                        |       |         |    |     |
|-------|------------------------|-------|---------|----|-----|
| Title |                        |       | USB 3.0 |    |     |
| Size  | Document Number        | Rev   |         |    |     |
| A3    | Latitude300 Haswell    | X00   |         |    |     |
| Date: | Friday, April 19, 2013 | Sheet | 34      | of | 104 |



## Right USB Power x1



<Core Design>



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Title

**USB Power SW**

Size

Document Number

**Latitude300 Haswell**

Rev

**X00**

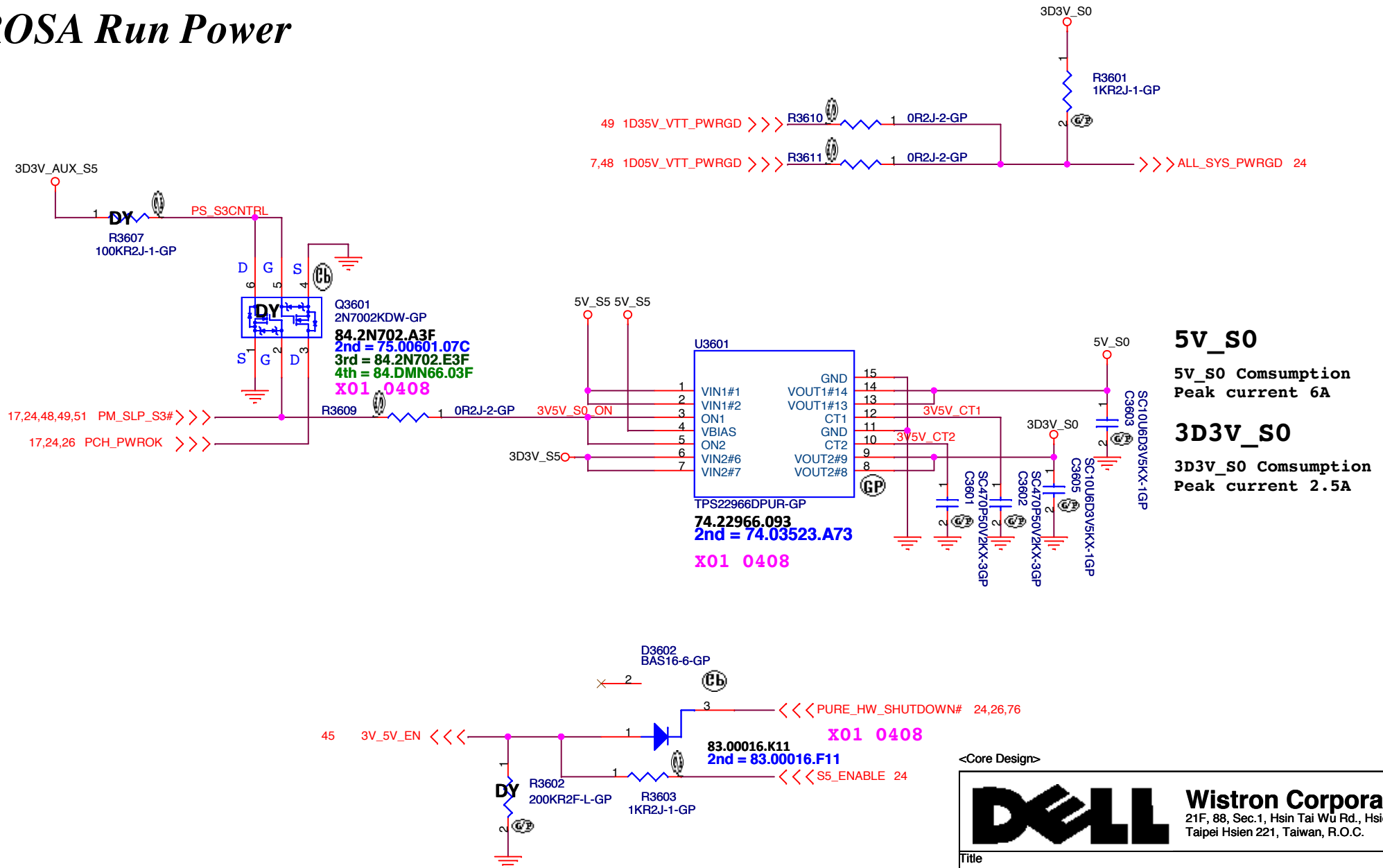
Date: Friday, April 19, 2013

Sheet 35 of 104

SSID = Reset.Suspend

Power Good

ROSA Run Power



<Core Design>



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Title

Power Plane Enable

Size  
A4

Document Number

Latitude300 Haswell

Rev

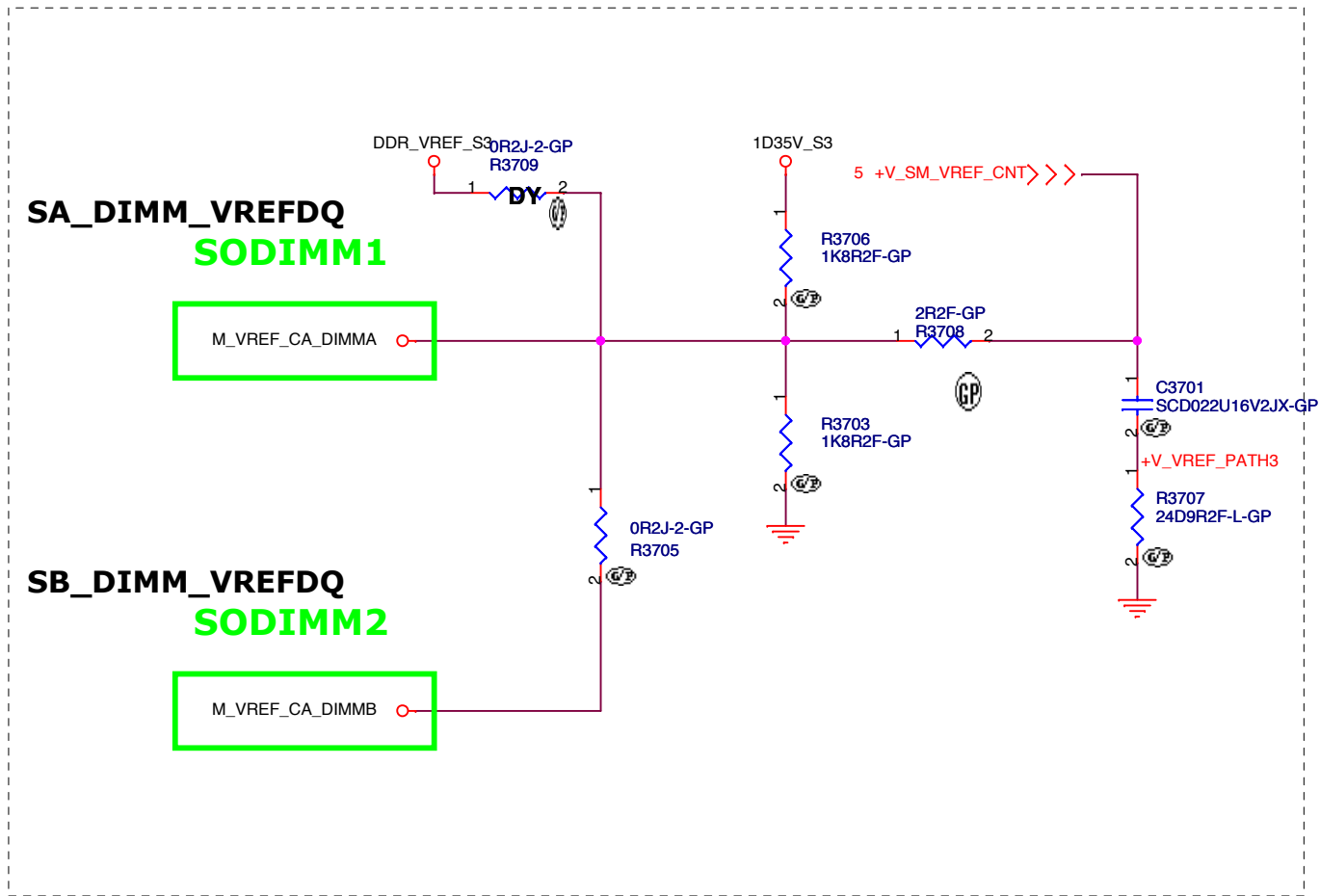
X00

Date: Friday, April 19, 2013

Sheet 36 of 104

**Layout Note:**

Place Close SO-DIMM



<Core Design>



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Title

**S3 Reduction Circuit**

Size  
A4

Document Number

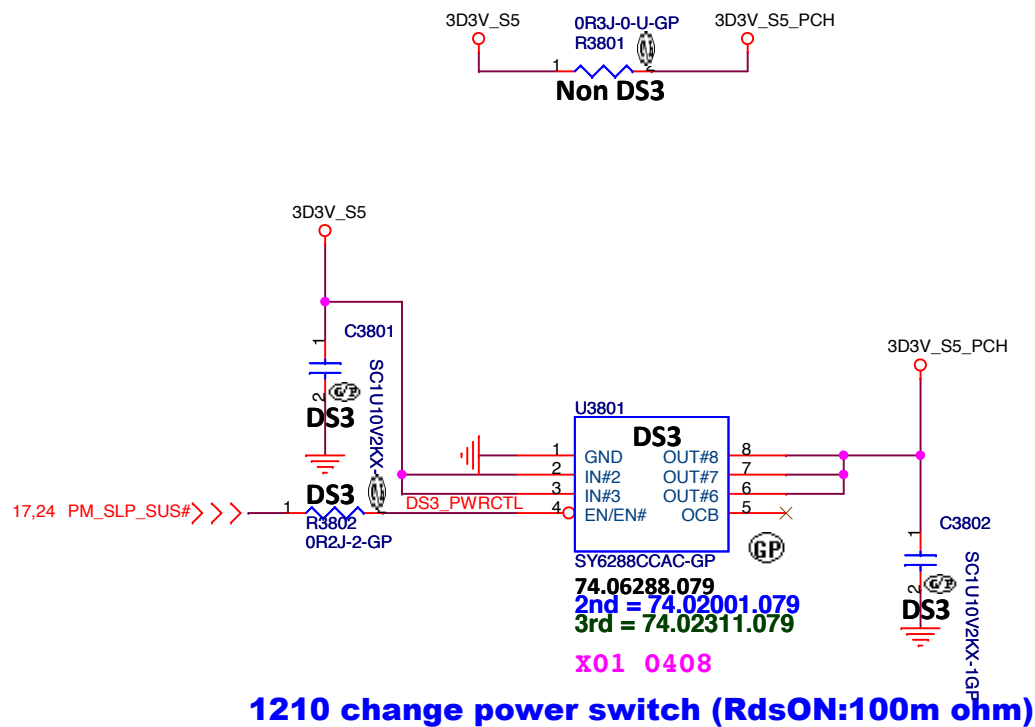
**Latitude300 Haswell**

Rev

**X00**

Date: Friday, April 19, 2013

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<Core Design>



**Wistron Corporation**  
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Title

**DSW**

Size  
A4

Document Number

**Latitude300 Haswell**


Rev  
**X00**

Date: Friday, April 19, 2013

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SSID = CPU

<Core Design>



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Title

CPU (POWER1)

|        |                     |     |
|--------|---------------------|-----|
| Size   | Document Number     | Rev |
| Custom | Latitude300 Haswell | X00 |

|                               |                 |
|-------------------------------|-----------------|
| Date: Tuesday, March 26, 2013 | Sheet 39 of 104 |
|-------------------------------|-----------------|


<Core Design>

|   |  |   |                          |
|---|--|---|--------------------------|
|  |  | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                          |
| Title   |  |   |                          |
| <b><i>Reserved</i></b>  |  |   |                          |
| Size<br>A3  | Document Number<br><b><i>Latitude300 Haswell</i></b> |   | Rev<br><b><i>X00</i></b> |
| Date: Tuesday, March 26, 2013   |  | Sheet 40 of   | 104                      |



(Blanking)

<Core Design>



**Wistron Corporation**  
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Title

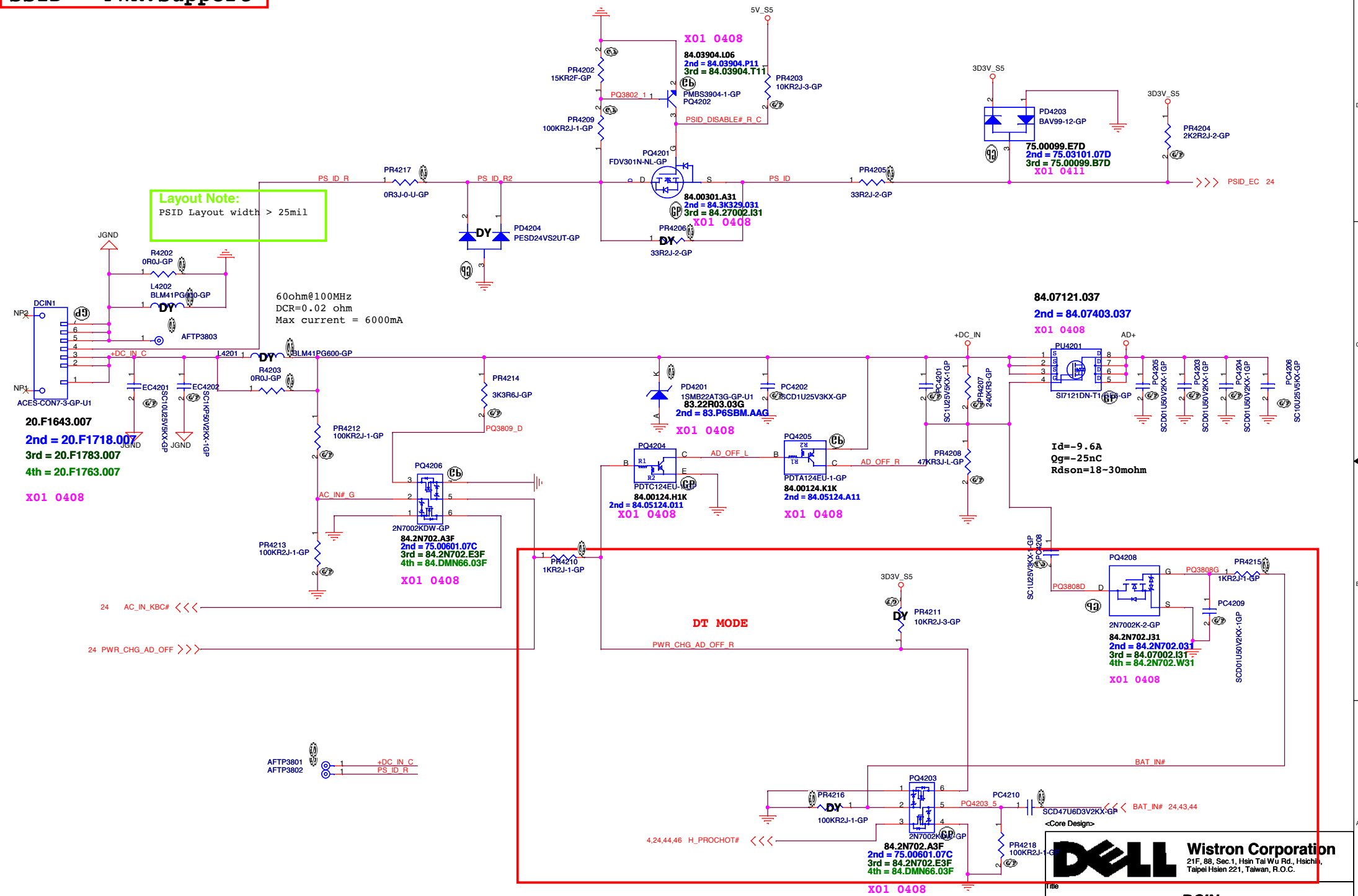
**Reserved**

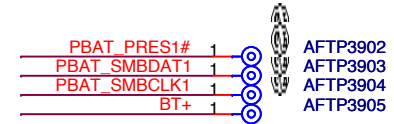
|      |                            |            |
|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                 |
|-------------------------------|-----------------|
| Date: Tuesday, March 26, 2013 | Sheet 41 of 104 |
|-------------------------------|-----------------|

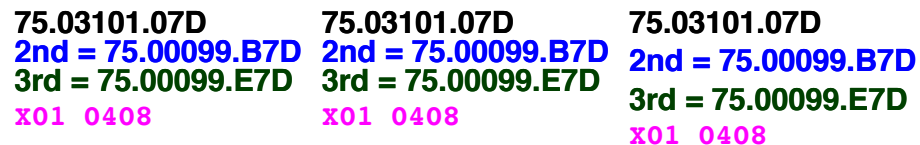
# SSID = PWR.Support

**Layout Note:**  
PSID Layout width > 25mil



**SSID = PWR.Support**

**Placement: Close to Batt Connector**



## <Core Design>

[illegible]

**BATT CONN**

Size  
A4

|                 |
|-----------------|
| Document Number |
|-----------------|

## Latitude300 Haswell

Rev  
voo

Date: Friday, April 19, 2013

|       |    |    |     |
|-------|----|----|-----|
| Sheet | 43 | of | 104 |
|-------|----|----|-----|

SSID = Charger

| REGN REGULATOR |                        |  |     |   |
|----------------|------------------------|--|-----|---|
| VREGN_RE       | REGN Regulator Voltage | VVCC = 6.5V, VACDET=0.6V (0-50mA load) | 5.5 | 6 |
| G              |                        |  | 6.5 | V |

KBC FOR DT MODE  
CHECK EE PULL HIGH

DIS\_DTM:  
H= cell is plus to GND. (reset charger ic)  
L=normal

CHECK EE

X01 Remove 15V\_S5, dummy  
the related parts 0409

CHECK EE  
follow customer circuits.

Close PR4443

CHECK PM BATTERY TYPE  
CHECK CELL for DT mode

Follow customer circuits

CHECK PM ADAPTER TYPE  
And setting adapter type

| ADAPTER TYPE | AD_IA_HW | AD_IA_HW_2 | SETTING   |
|--------------|----------|------------|-----------|
| 90W          | L        | L          | 1.099V    |
| 65W          | H        | L          | 0.862329V |
| 45W          | L        | H          | 0.659648V |

•Core Design:

**DELL** Wistron Corporation  
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Taichung 305, Taiwan, R.O.C.

**CHARGER BQ24717**

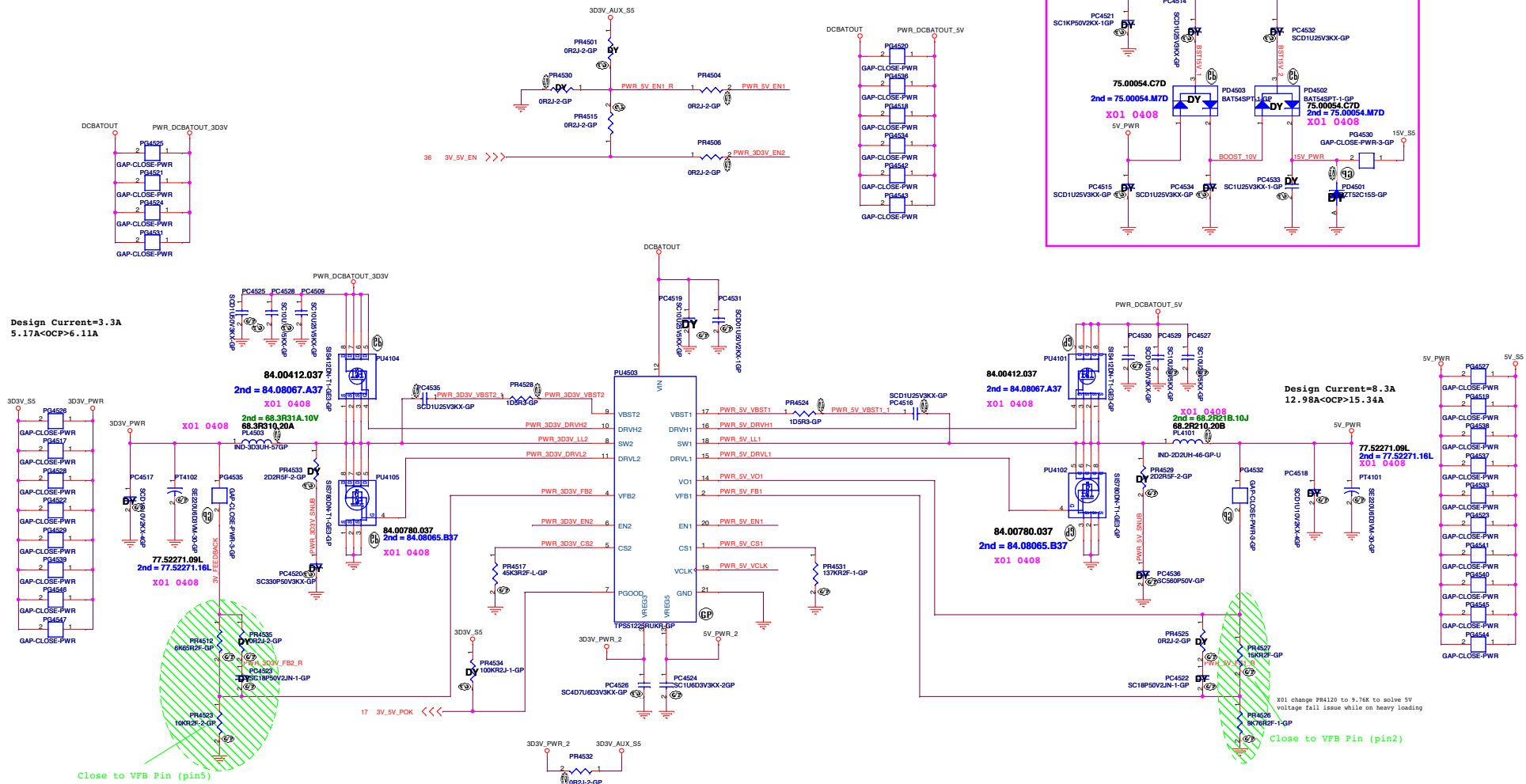
|     |      |        |     |
|-----|------|--------|-----|
| Rev | Docu | Number | Rev |
| 1.0 | 1.0  | 1.0    | 1.0 |

Latitude300 Haswell

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```
SSID = PWR.Plane.Regulator_5v3p3v
```



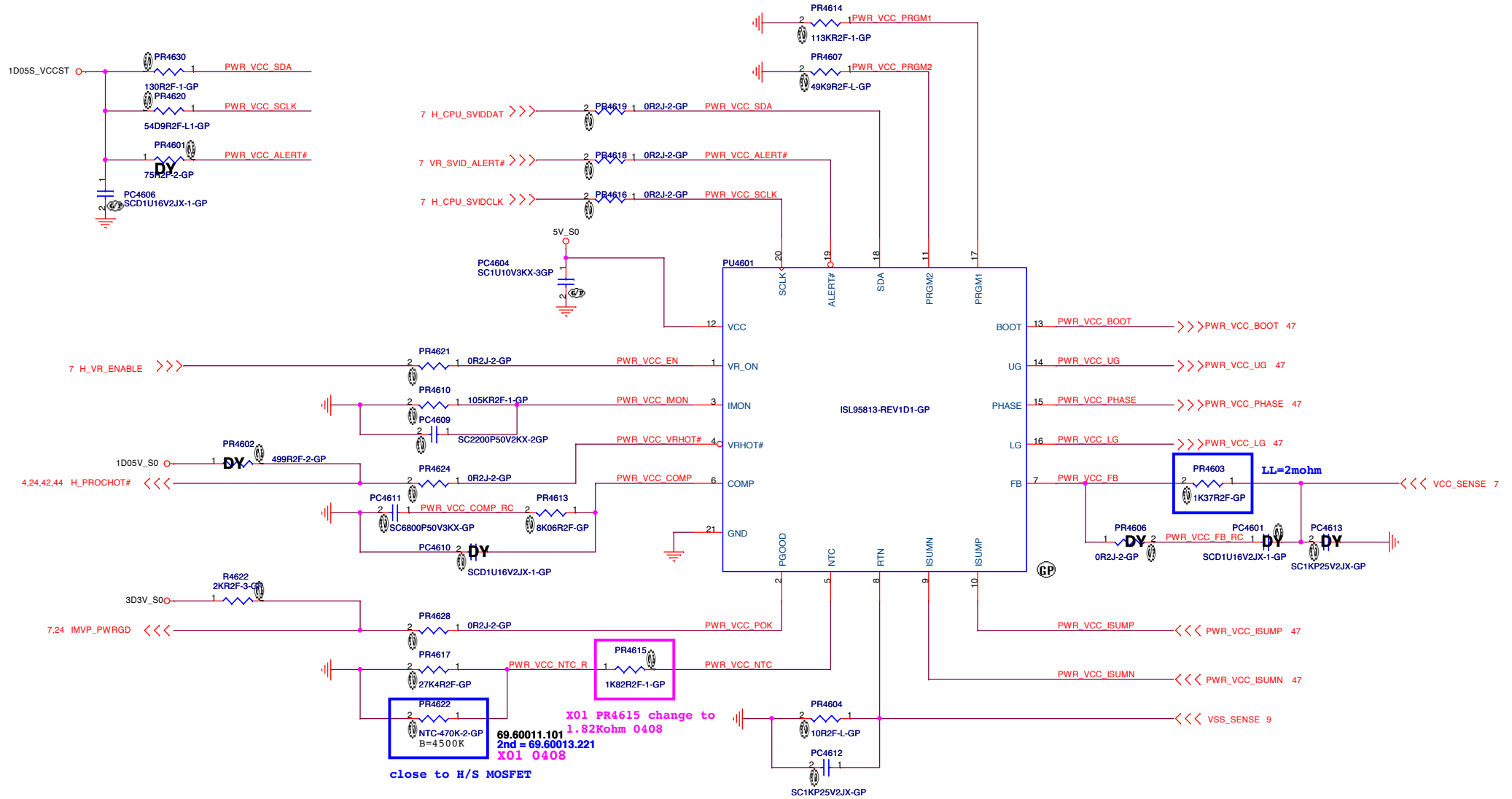
I/P cap: CHIP CAP C 10.25V X0805 X5R/ 78.10622.51L  
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap:CHIP CAP POL 220U 6.3V M 6.3\*4.5 /Matsuki/ 17mOhm / 77.52271.09L  
H/S:SI8142 / 24mOhm/30mOhm#4.5Vgs / 84.00412.037  
L/S:SI8780 / 14.5mOhm/17.5mOhm#4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-lay

|        |          |          |
|--------|----------|----------|
|        | TPS51225 | TPS51285 |
| PR4510 | 45.3KK   | 9.09K    |
| PR4511 | 110K     | 22.1K    |

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 18.10622.51L  
Inductor: CHIP CHOK 2.2U PCMC063T 2R2M 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap:CHIP CAP POL 220U 6.3V M 6.3\*4.5 /Matsuki/ 17mOhm / 77.52271.09L  
H/S:SIS412 / 24mOhm/30mOhmE4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhmE4.5Vgs / 84.00780.037

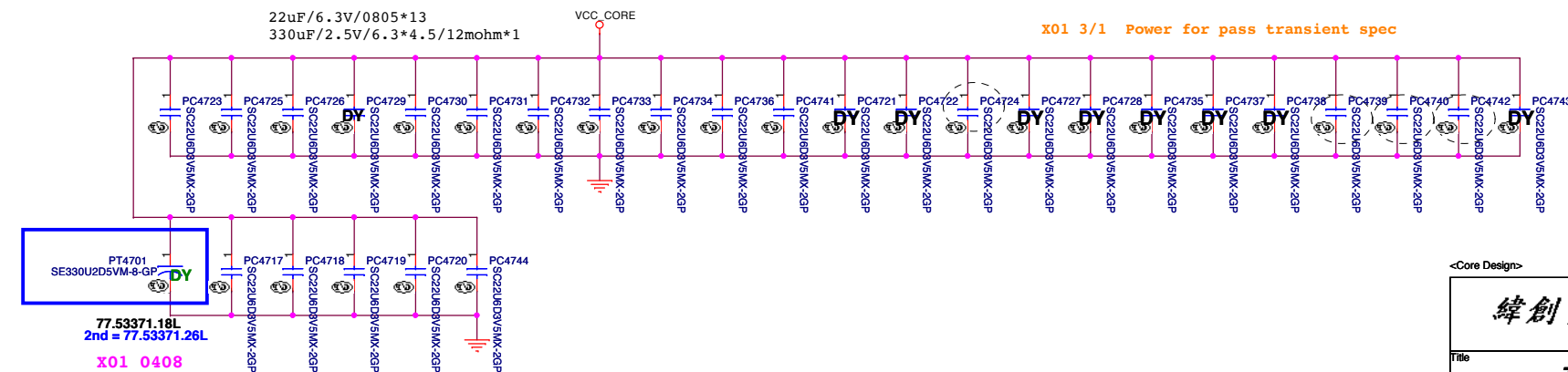
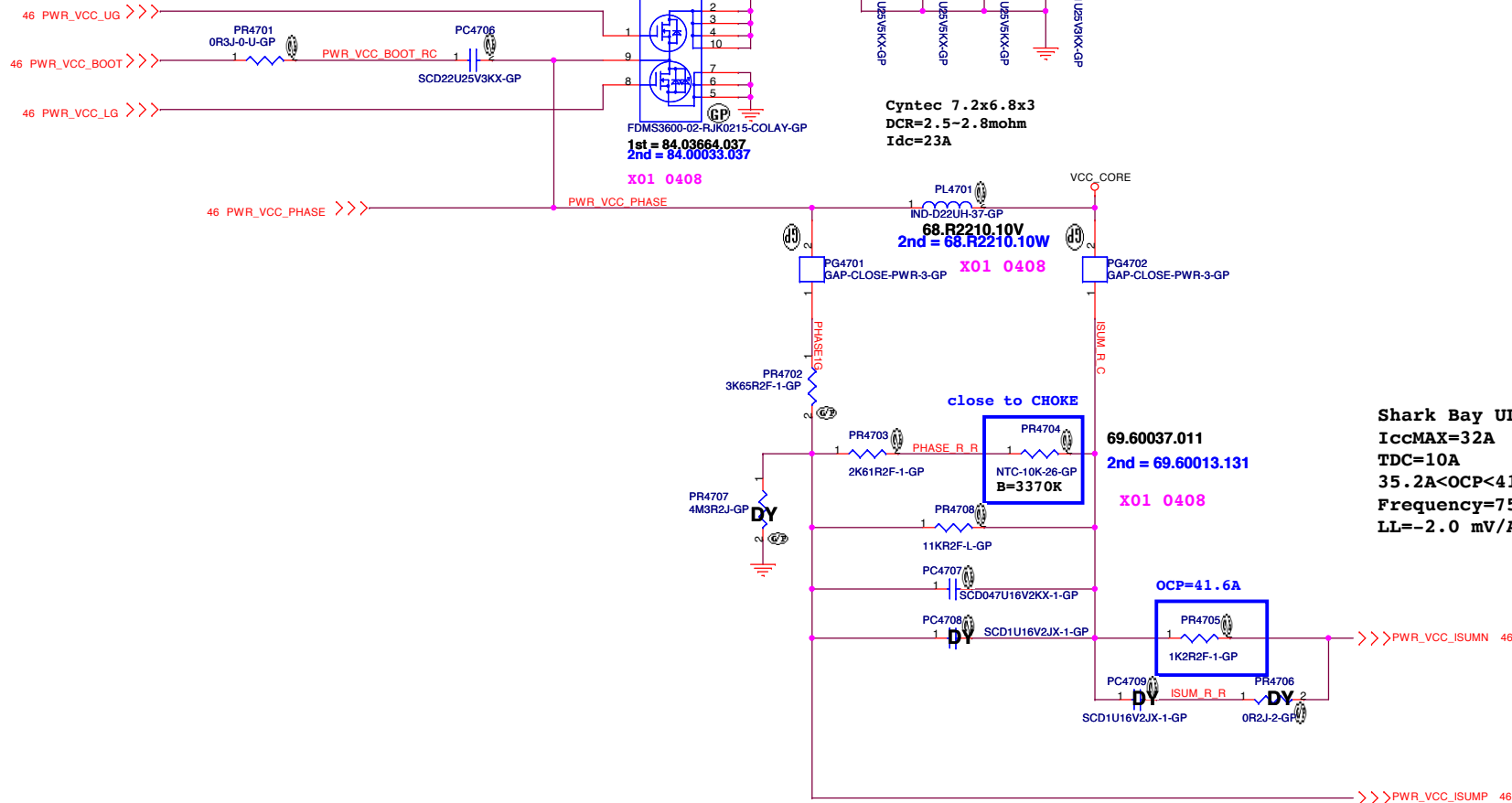
SSID = CPU.Regulator

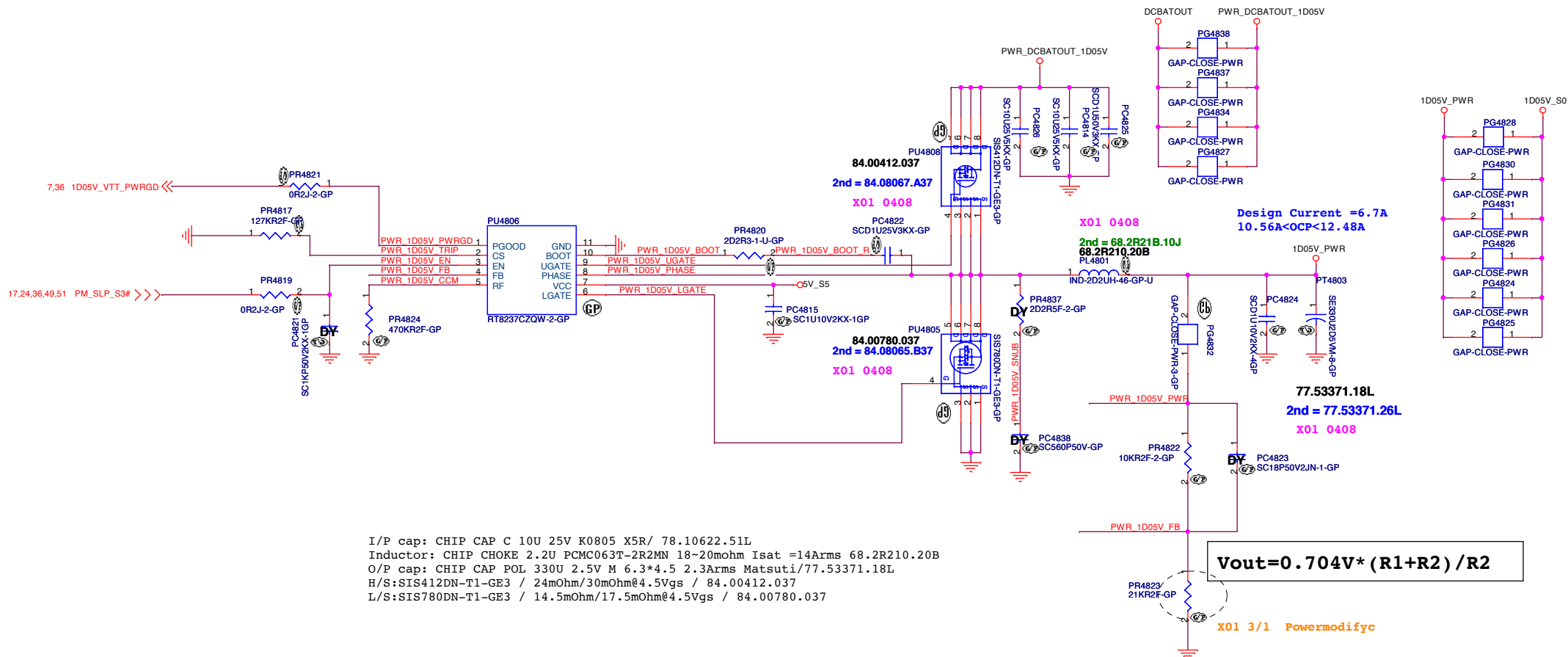


<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

| Title                        |                 |            |
|------------------------------|-----------------|------------|
| TPS51622 CPUCORE(1/2)        |                 |            |
| Size<br>A3                   | Document Number | Rev<br>X00 |
| Latitude300 Haswell          |                 |            |
| Date: Friday, April 19, 2013 | Sheet 46 of 104 |            |



**SSID = PWR.Plane.Regulator\_1p05v**

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**TPS51367 1D05V**Size  
A

Document Number

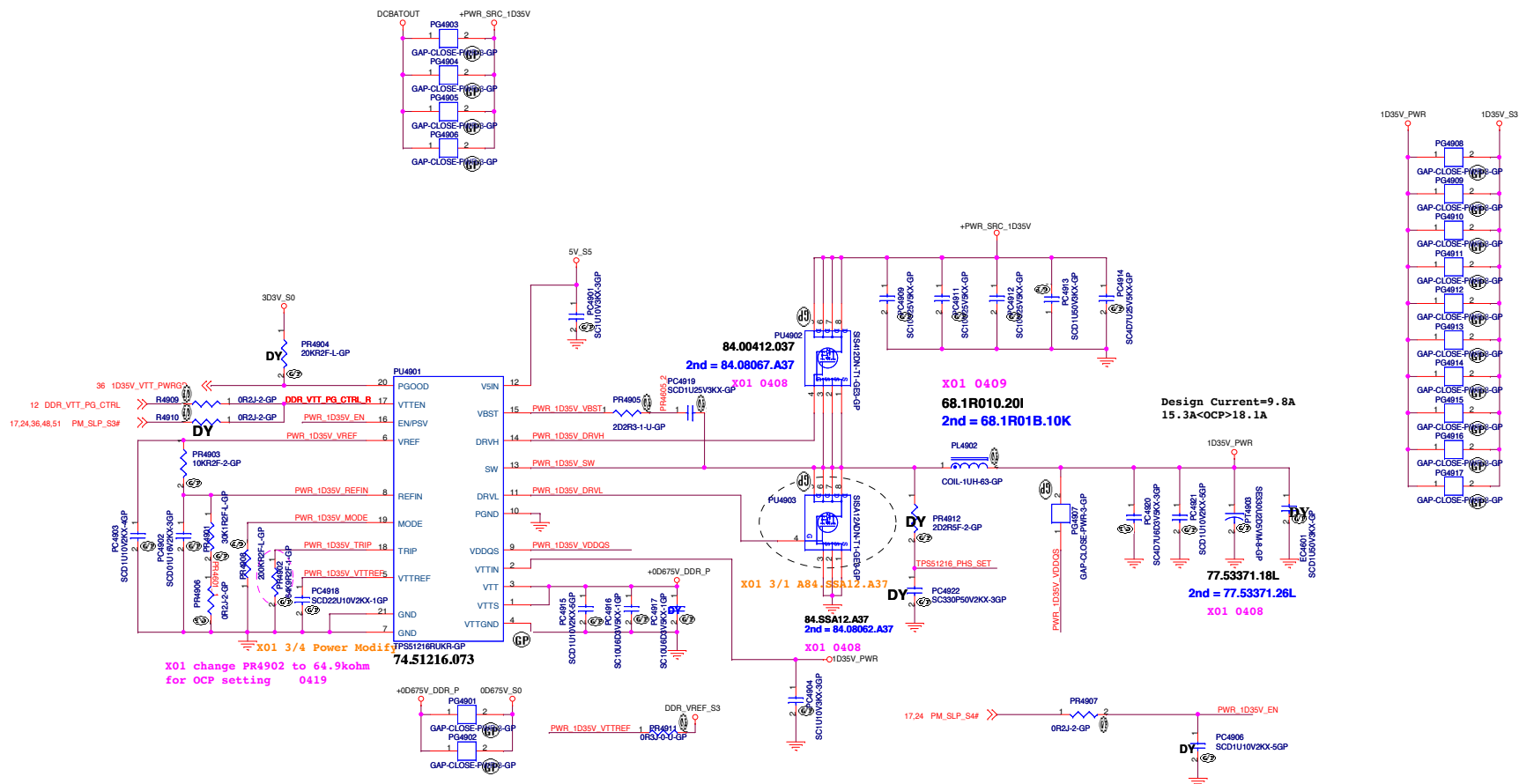
|     |   |
|-----|---|
| Rev | Y |
|-----|---|

Date: Friday, April 19, 2013

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SSID = PWR.Plane.Regulator 1p35v0p675v



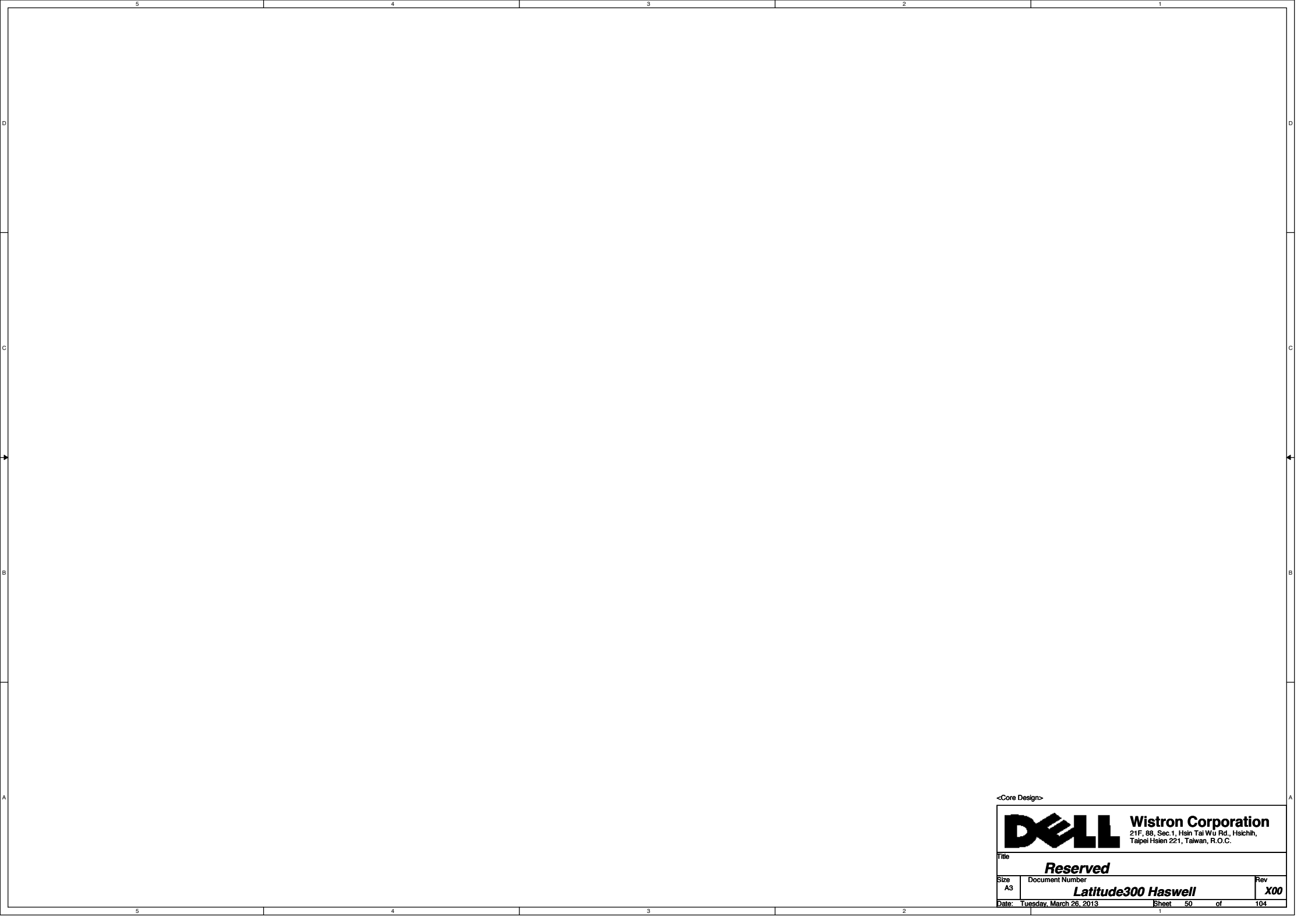
| State | S3 | S5 | VDDR | VTTREF | VTT        |
|-------|----|----|------|--------|------------|
| S0    | Hi | Hi | On   | On     | On         |
| S3    | Lo | Hi | On   | On     | Off (Hi-Z) |
| S4/S5 | Lo | Lo | Off  | Off    | Off        |

**MODE**


|          |           |                        |
|----------|-----------|------------------------|
| PR4608   | Frequency | Discharge Mode         |
| 200k ohm | 400kHz    | Tracking Discharge     |
| 100k ohm | 300kHz    |                        |
| 68k ohm  | 300kHz    | Non-tracking Discharge |
| 47k ohm  | 400kHz    |                        |

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP IND 0.1UH M PCMC063T-R10NN 1.5-1.7mohm Isat =60Arms 68.R1010.10T  
O/P cap: CHIP CAP POL 330U 2.5V M 6.34V 5 2.3Arms Matsuti/77.53371.18L  
H/S MOS: FET MOS ISi412DN-T1-GE3 NC RP / 84.00412.037 / Rds(on)=24-30mohm @Vgs=4.5V  
L/S MOS: FET MOS ISi780DN-T1-GE3 NC RP POWERPAK 121 / 84.00780.037 / Rds(on)=14.5-17.5mohm @Vgs=4.5V

<Core Design>



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

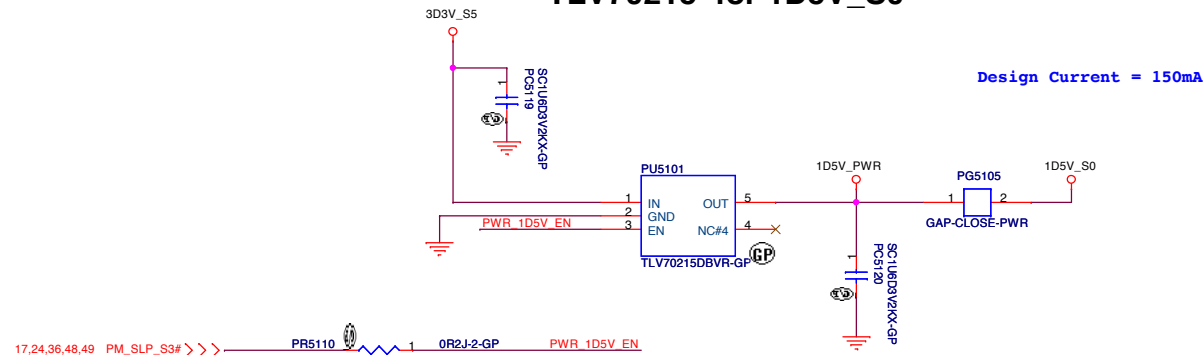
Title

***Reserved***

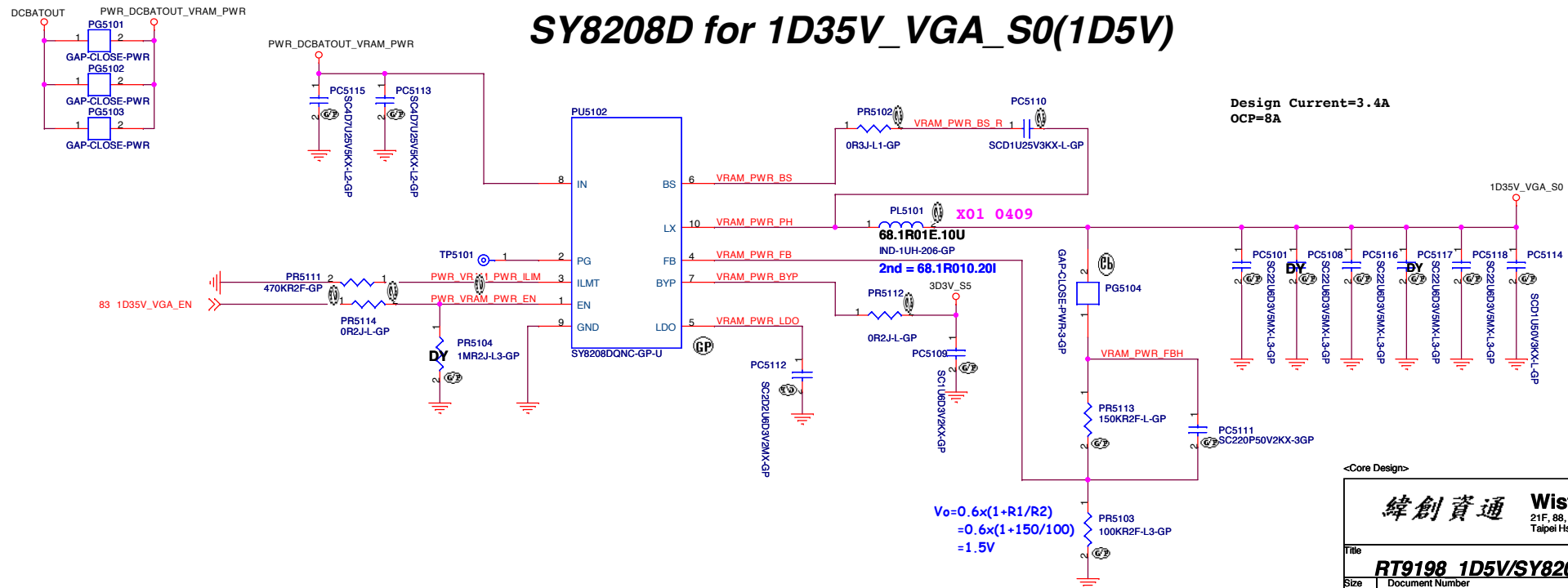
|       |                                   |                   |
|-------|-----------------------------------|-------------------|
| Size  | Document Number                   | Rev               |
| A3    | <b><i>Latitude300 Haswell</i></b> | <b><i>X00</i></b> |
| Date: | Tuesday, March 26, 2013           | Sheet 50 of 104   |

**SSID = PWR.Plane.Regulator\_1p5v**

## TLV70215 for 1D5V\_S0



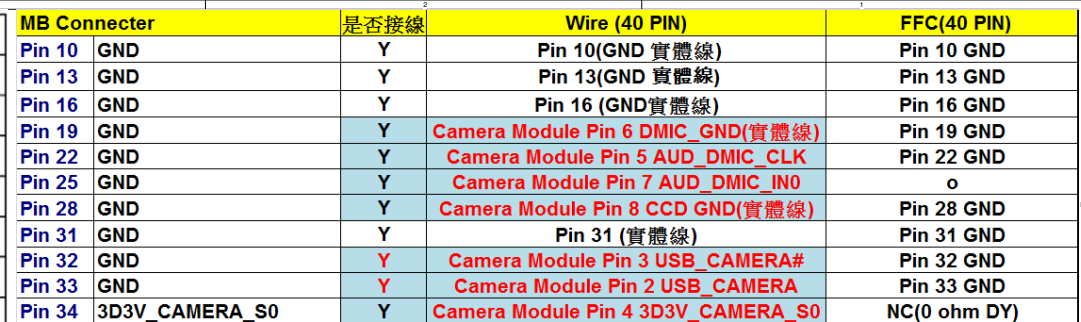
***SY8208D for 1D35V\_VGA\_S0(1D5V)***



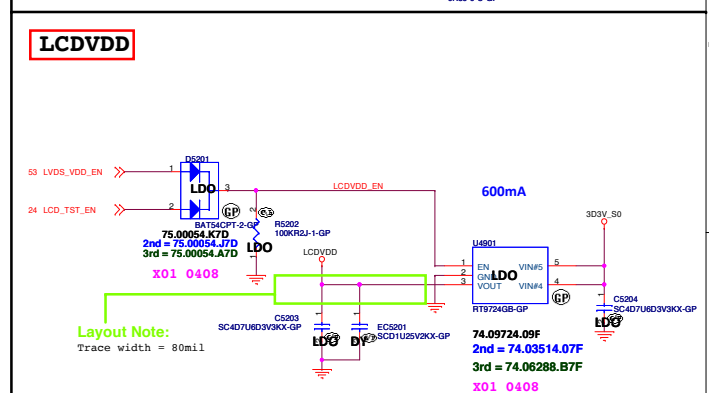
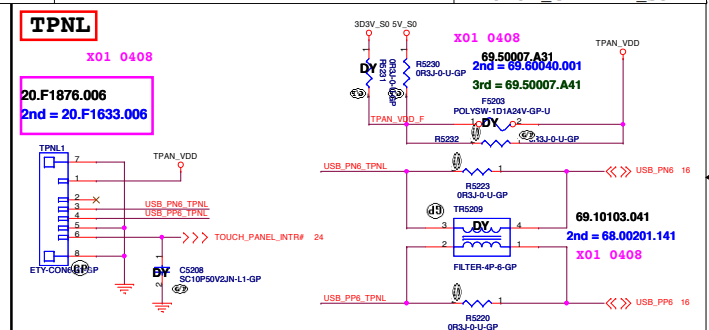
### <Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

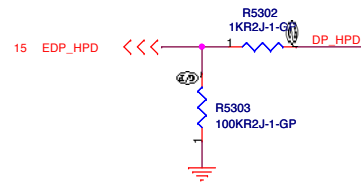
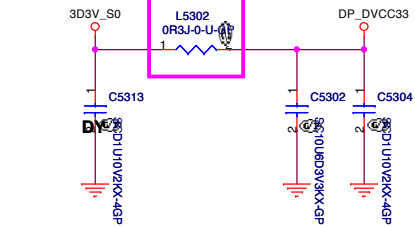
|                                      |                            |       |            |
|--------------------------------------|----------------------------|-------|------------|
| Title                                |                            |       |            |
| <b>RT9198 1D5V/SY8208D 1D5V(VGA)</b> |                            |       |            |
| Size                                 | Document Number            | Rev   |            |
| A3                                   | <b>Latitude300 Haswell</b> |       | <b>X00</b> |
| Date:                                | Friday, April 19, 2013     | Sheet | 51 of 104  |



| PIN | MB Connector         | 是否接線 | PIN | Camera Module Conn   |
|-----|----------------------|------|-----|----------------------|
| 1   | DGND                 | Y    | 8   | DGND                 |
| 2   | USB_CAMERA_C (USB+)  | Y    | 2   | USB_CAMERA_C (USB+)  |
| 3   | USB_CAMERA#_C (USB-) | Y    | 3   | USB_CAMERA#_C (USB-) |
| 4   | DMIC_GND             | Y    | 6   | DMIC_GND             |
| 5   | DMIC_CLK_C           | Y    | 5   | DMIC_CLK_C           |
| 6   | DMIC_DATA_C          | Y    | 7   | DMIC_DATA_C          |
| 7   | NC                   | N    | 1   | NC                   |
| 8   | 3D3V CAMERA S0       | Y    | 4   | 3D3V CAMERA S0       |



X01 Change L5301 L5302 to 0ohm resistor, DY C5301 0410



24 L\_BKLT\_EN  
52 LVDS\_DDC\_DATA\_R  
52 LVDS\_DDC\_CLK\_R

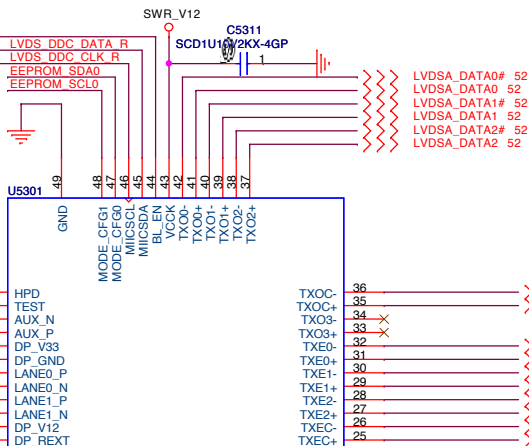
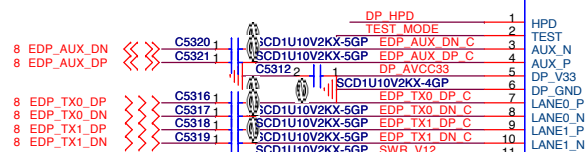
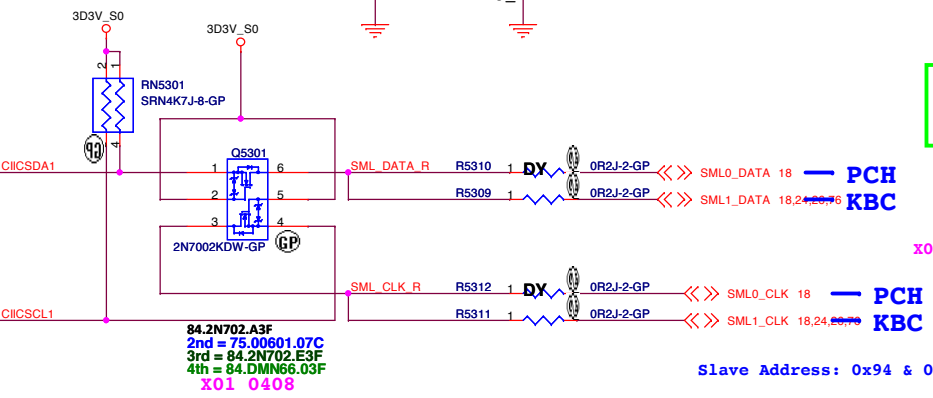
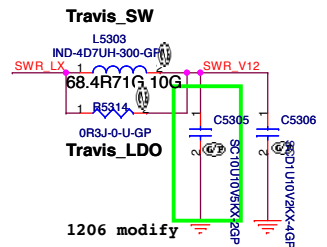
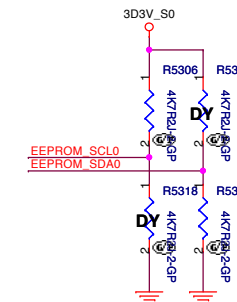


Table 2 Operation Mode Table

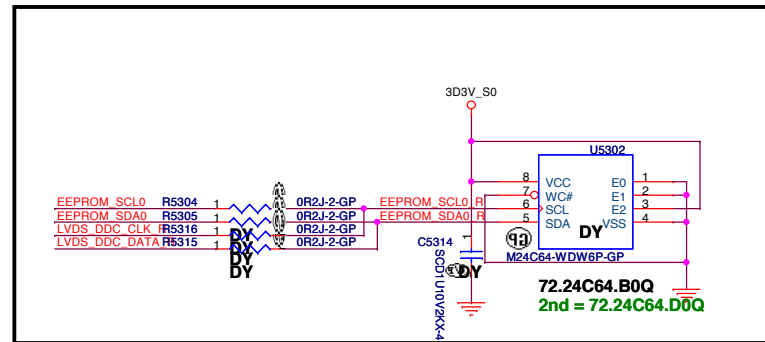
| PIN48 | PIN47 |         |
|-------|-------|---------|
|       | 0     | 1       |
| 0     | X     | EP Mode |
| 1     | ROM   | EEPROM  |



X01 DY C5307 0410

Close to PIN13

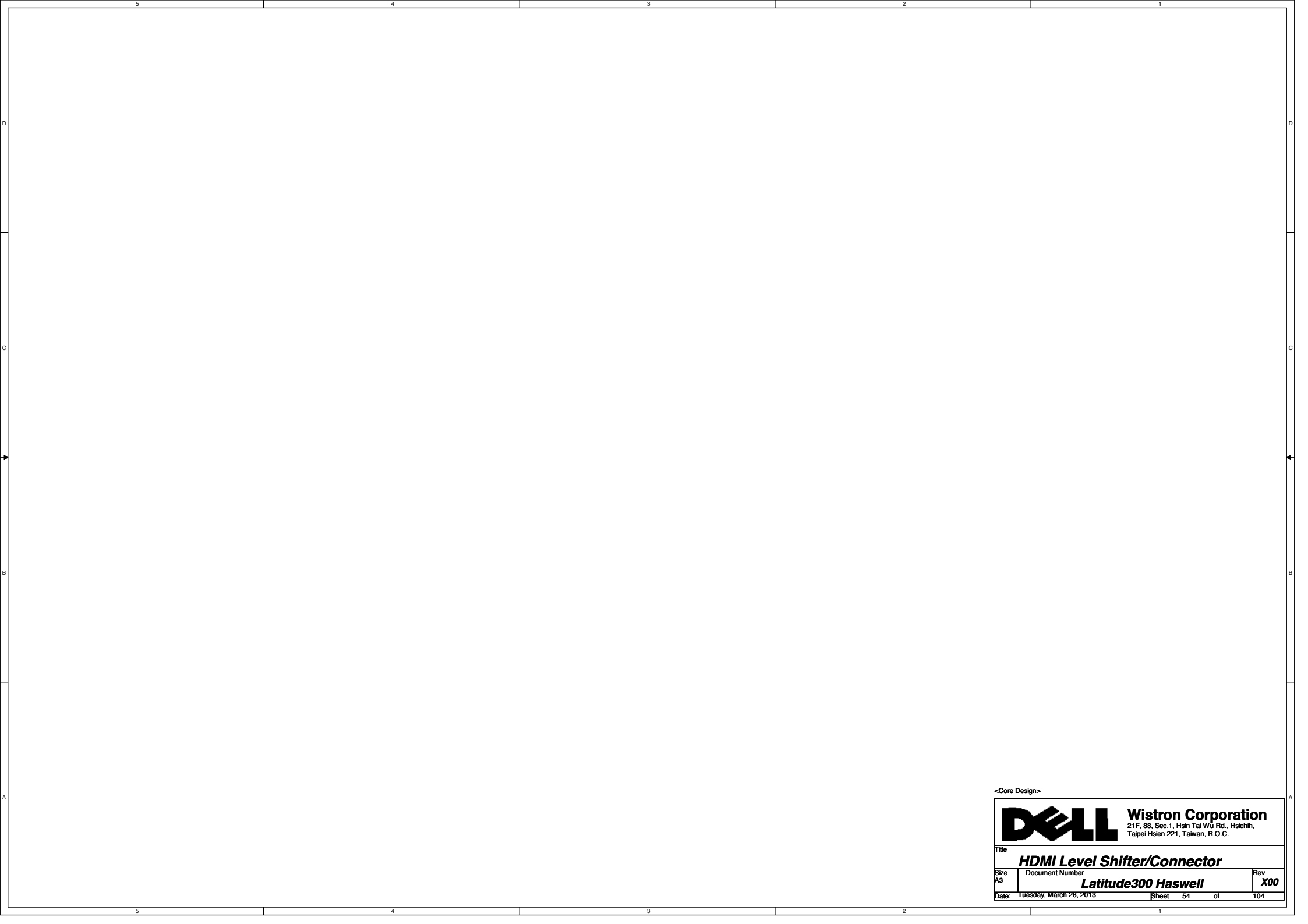
## EEPROM



<Core Design>

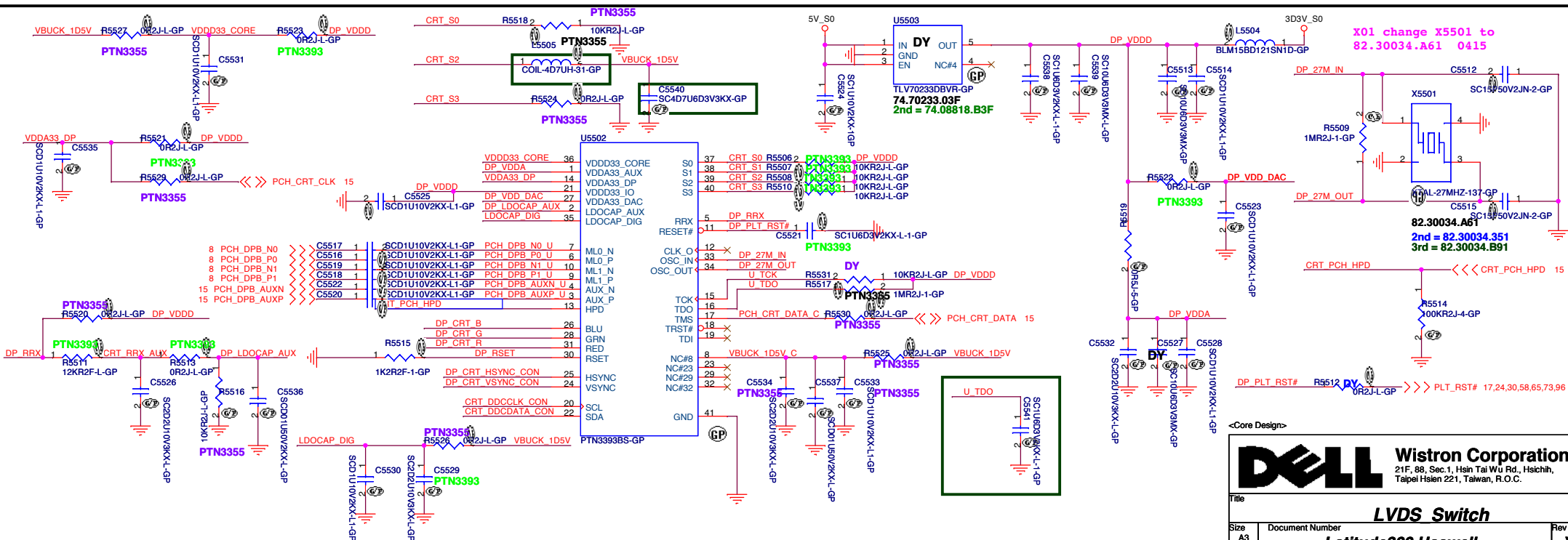
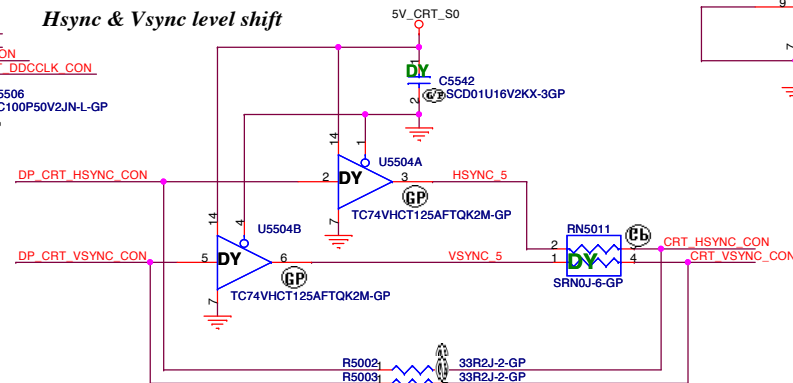
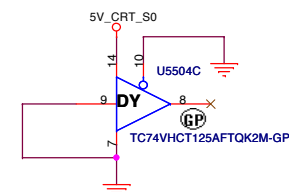
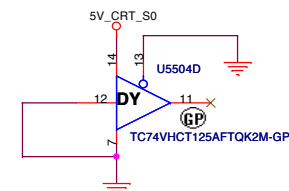
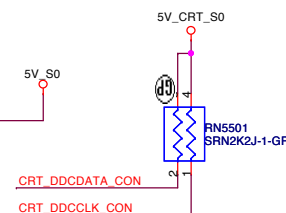
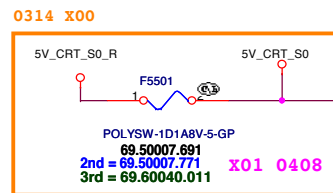
**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

| Title                        |                 |         |
|------------------------------|-----------------|---------|
| LVDS Switch                  |                 |         |
| Size A3                      | Document Number | Rev X00 |
| Latitude300 Haswell          |                 |         |
| Date: Friday, April 19, 2013 | Sheet 53 of 104 |         |



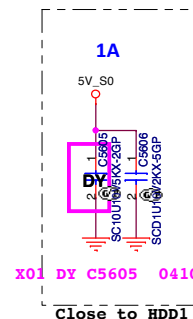
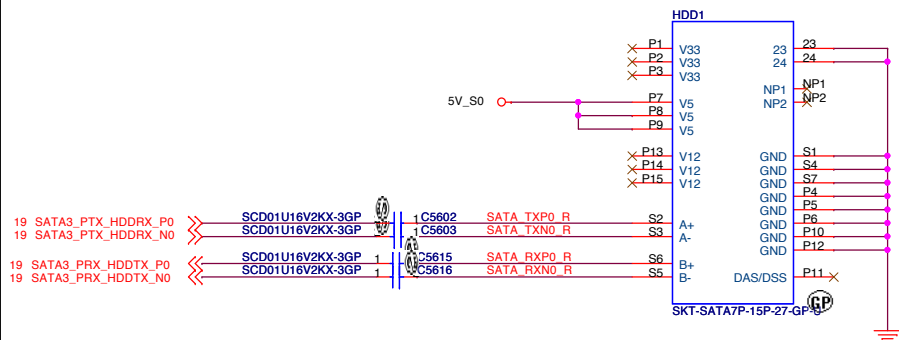
<Core Design>

|   |                            |   |            |
|---|----------------------------|---|------------|
|  |                            | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |            |
| Title   |                            |   |            |
| <b>HDMI Level Shifter/Connector</b>   |                            |   |            |
| Size  | Document Number            |   | Rev        |
| A3  | <b>Latitude300 Haswell</b> |   | <b>X00</b> |
| Date:   | Tuesday, March 26, 2013    | Sheet   | 54 of 104  |

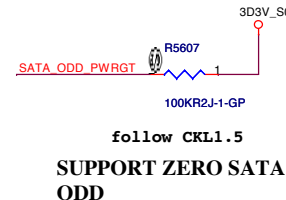
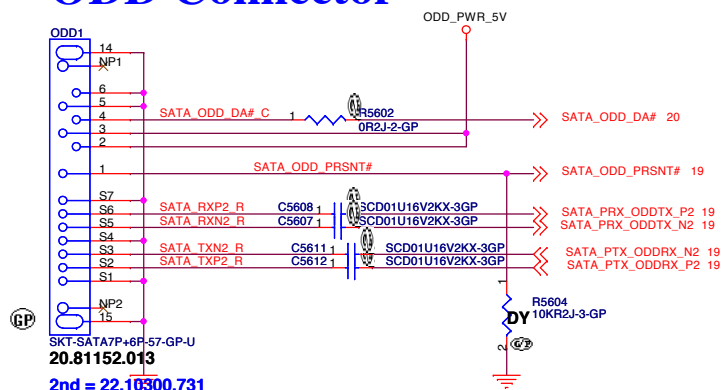
[illegible]

SSID = SATA

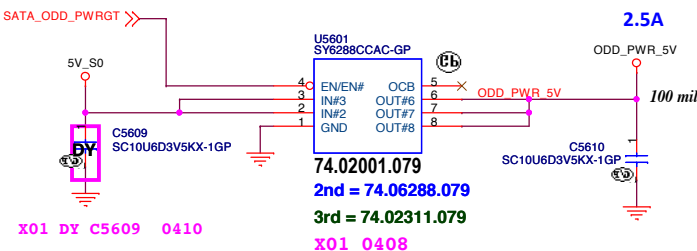
## SATA HDD Connector



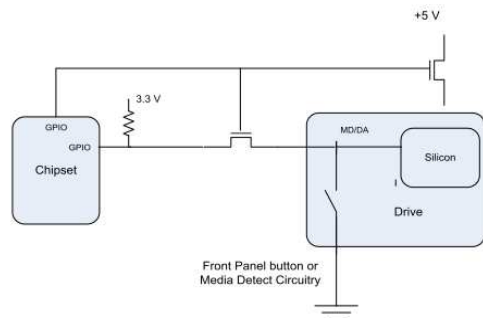
## ODD Connector



## SATA Zero Power ODD



Current limit  
Active High  
typ => 2.5A



<Core Design>


|                              |                 |   |     |
|------------------------------|-----------------|---|-----|
| <b>DELL</b>                  |                 | <b>Wistron Corporation</b>  |     |
|                              |                 | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |     |
| Title                        |                 |   |     |
| <b>HDD/ODD</b>               |                 |   |     |
| Size<br>A3                   | Document Number |   | Rev |
| <b>Latitude300 Haswell</b>   |                 | <b>X00</b>  |     |
| Date: Friday, April 19, 2013 | Sheet 56        | of 104  |     |



SSID = ESATA

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<Core Design>



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Title

**ESATA**

Size  
A3

Document Number  
**Latitude300 Haswell**

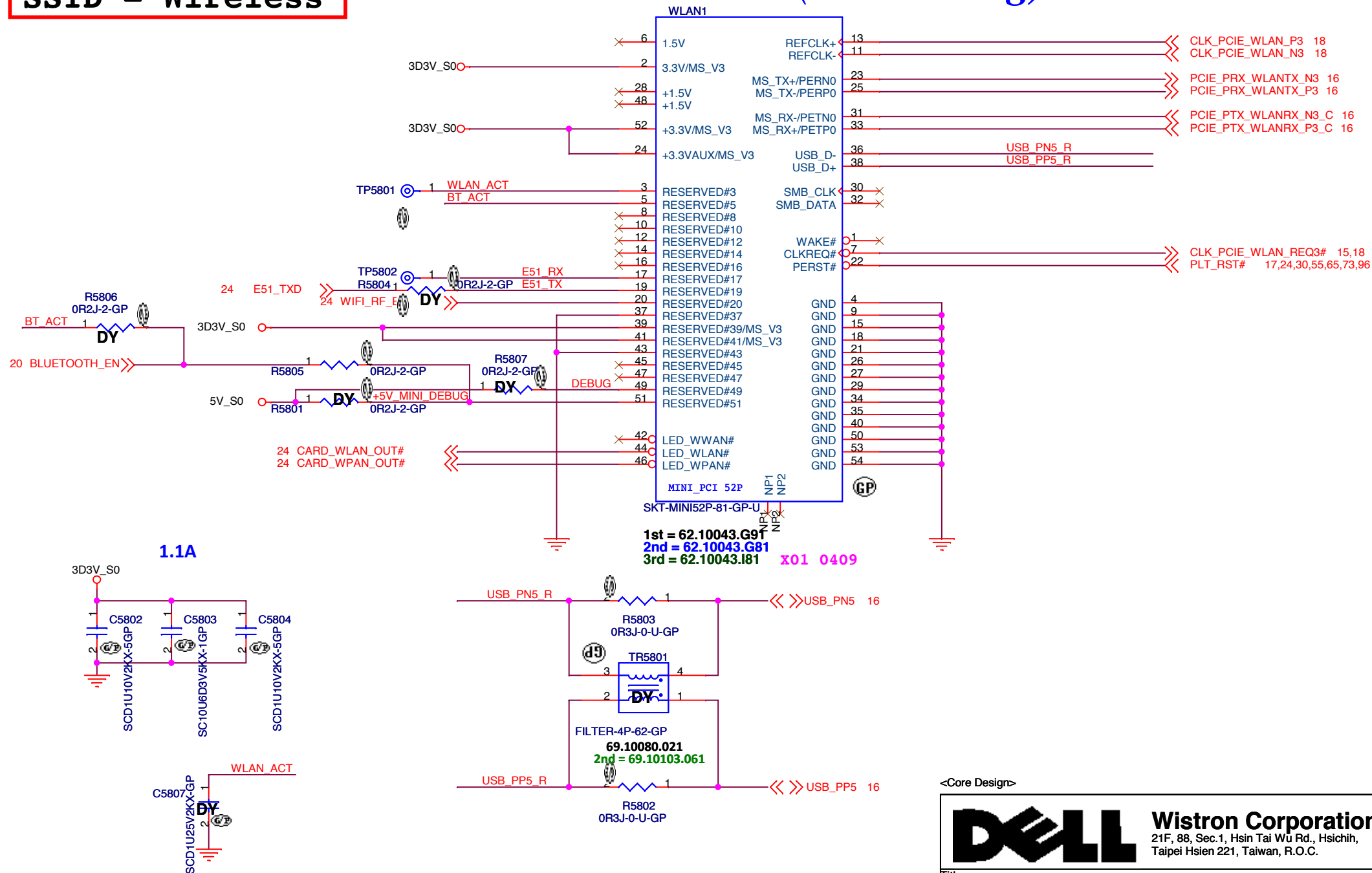
Rev  
**X00**

Date: Tuesday, March 26, 2013

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SSID = Wireless

# Mini Card Connector(802.11a/b/g)



<Core Design>



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Title

**MINICARD(WLAN)/MTP CONN**

Size  
A4

Document Number

**Latitude300 Haswell**

Rev


**X00**

Date: Friday, April 19, 2013

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<Core Design>



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Title

**Reserved**

|      |                            |            |
|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                 |
|-------------------------------|-----------------|
| Date: Tuesday, March 26, 2013 | Sheet 59 of 104 |
|-------------------------------|-----------------|

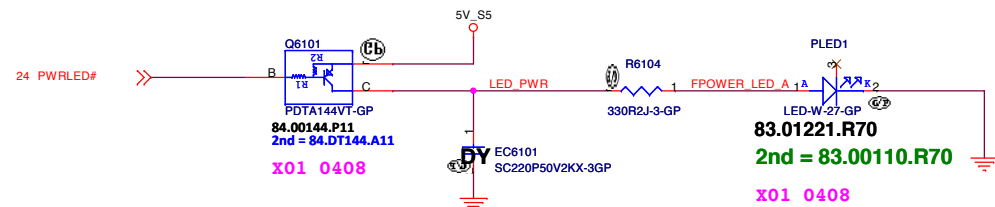
SSID = PCH

<Core Design>

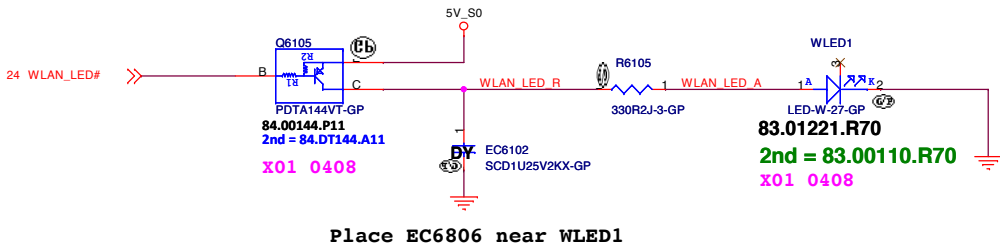
|   |   |   |                   |
|---|---|---|-------------------|
|  |   | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title (Reserved)  |   |   |                   |
| Size<br>A4  | Document Number<br><b>Latitude300 Haswell</b> |   | Rev<br><b>X00</b> |
| Date: Tuesday, March 26, 2013   |   | Sheet 60 of   | 104               |

**SSID = User.Interface**

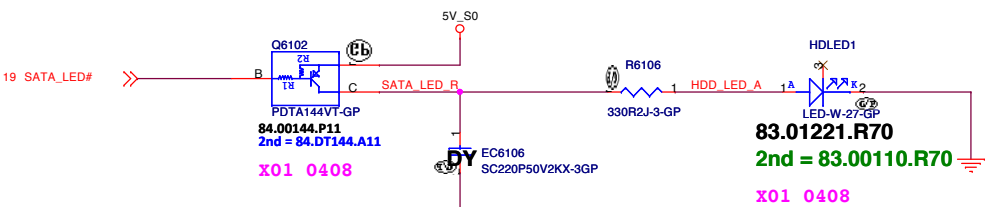
**FRONT POWER LED**  
Low actived from KBC GPIO



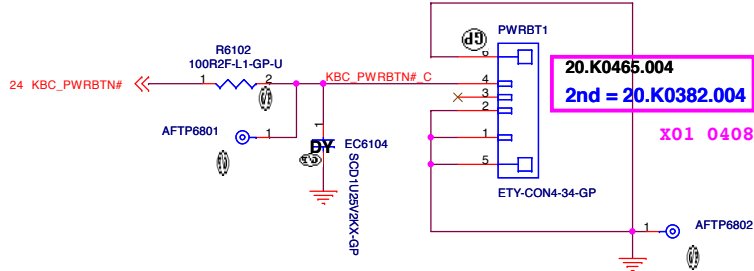
**Wireless LED**  
Low actived from KBC GPIO



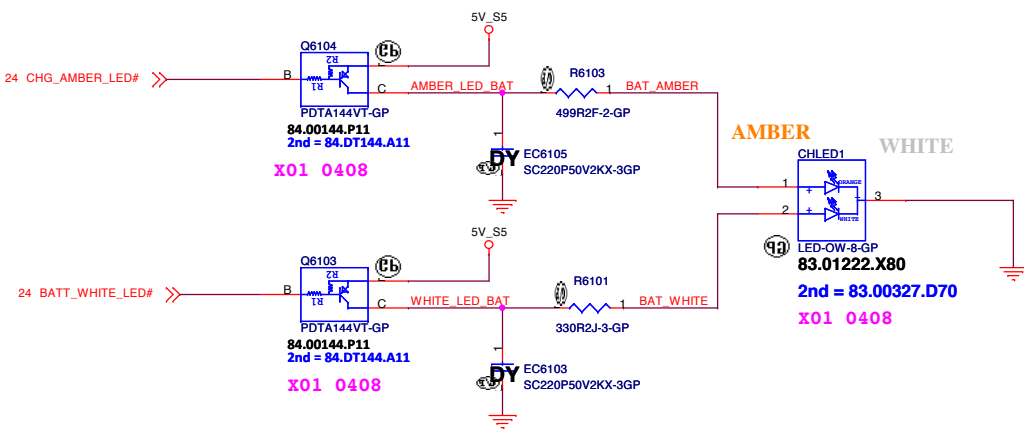
**SATA HDD LED(White)**  
Low actived from PCH GPIO



**Power button**



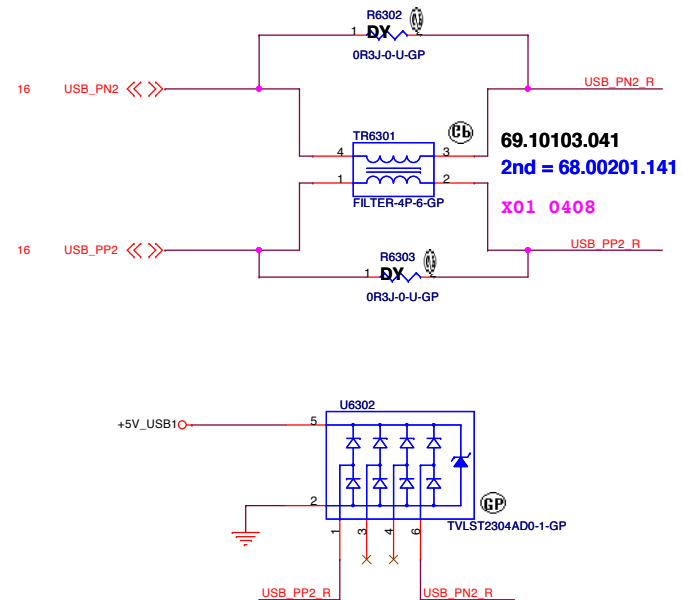
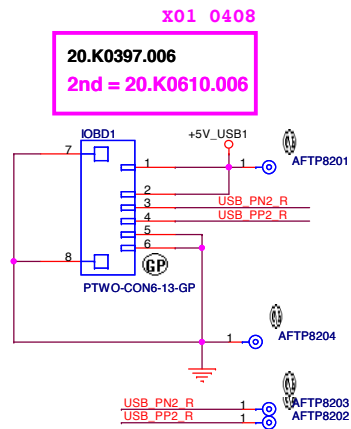
**Battery LED1 (AMBER\_LED)**  
Low actived from KBC GPIO



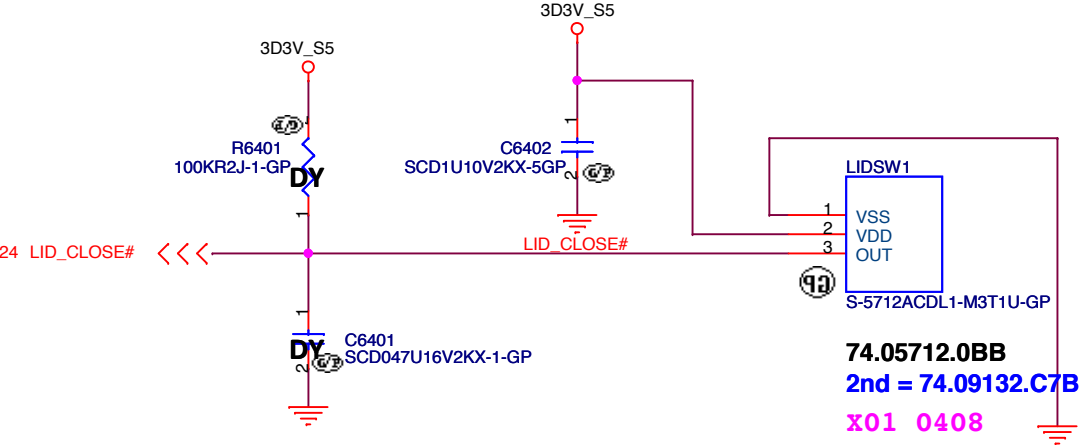
**Battery LED2 (WHITE\_LED)**  
Low actived from KBC GPIO




SSID = User.Interface



SSID = User.Interface

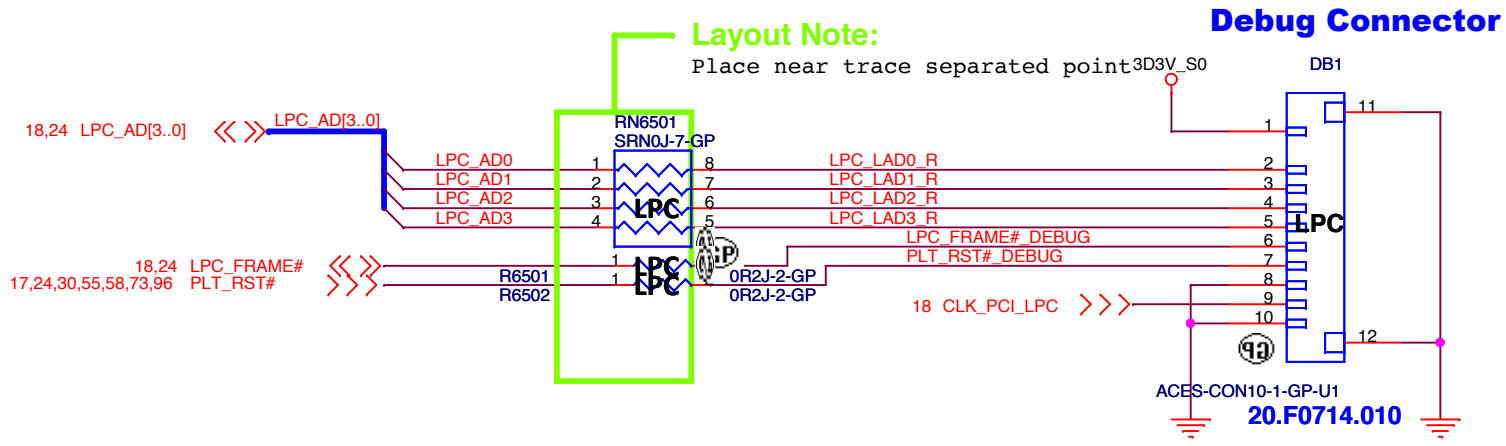


<Core Design>


|   |   |   |                   |
|---|---|---|-------------------|
|  |   | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title<br><b>Hall Sensor</b>   |   |   |                   |
| Size<br>A4  | Document Number<br><b>Latitude300 Haswell</b> |   | Rev<br><b>X00</b> |
| Date: Friday, April 19, 2013  |   | Sheet 64 of 104   |                   |



SSID = DEBUG PORT




<Core Design>

|   |   |   |                   |
|---|---|---|-------------------|
|  |   | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title<br><b>Dubug connector</b>   |   |   |                   |
| Size<br>A4  | Document Number<br><b>Latitude300 Haswell</b> |   | Rev<br><b>X00</b> |
| Date: Friday, April 19, 2013  |   | Sheet 65 of   | 104               |

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Title


**Reserved**

|      |                            |            |
|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                 |
|-------------------------------|-----------------|
| Date: Tuesday, March 26, 2013 | Sheet 66 of 104 |
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Title


**Reserved**

|      |                            |            |
|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                 |
|-------------------------------|-----------------|
| Date: Tuesday, March 26, 2013 | Sheet 67 of 104 |
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<Core Design>



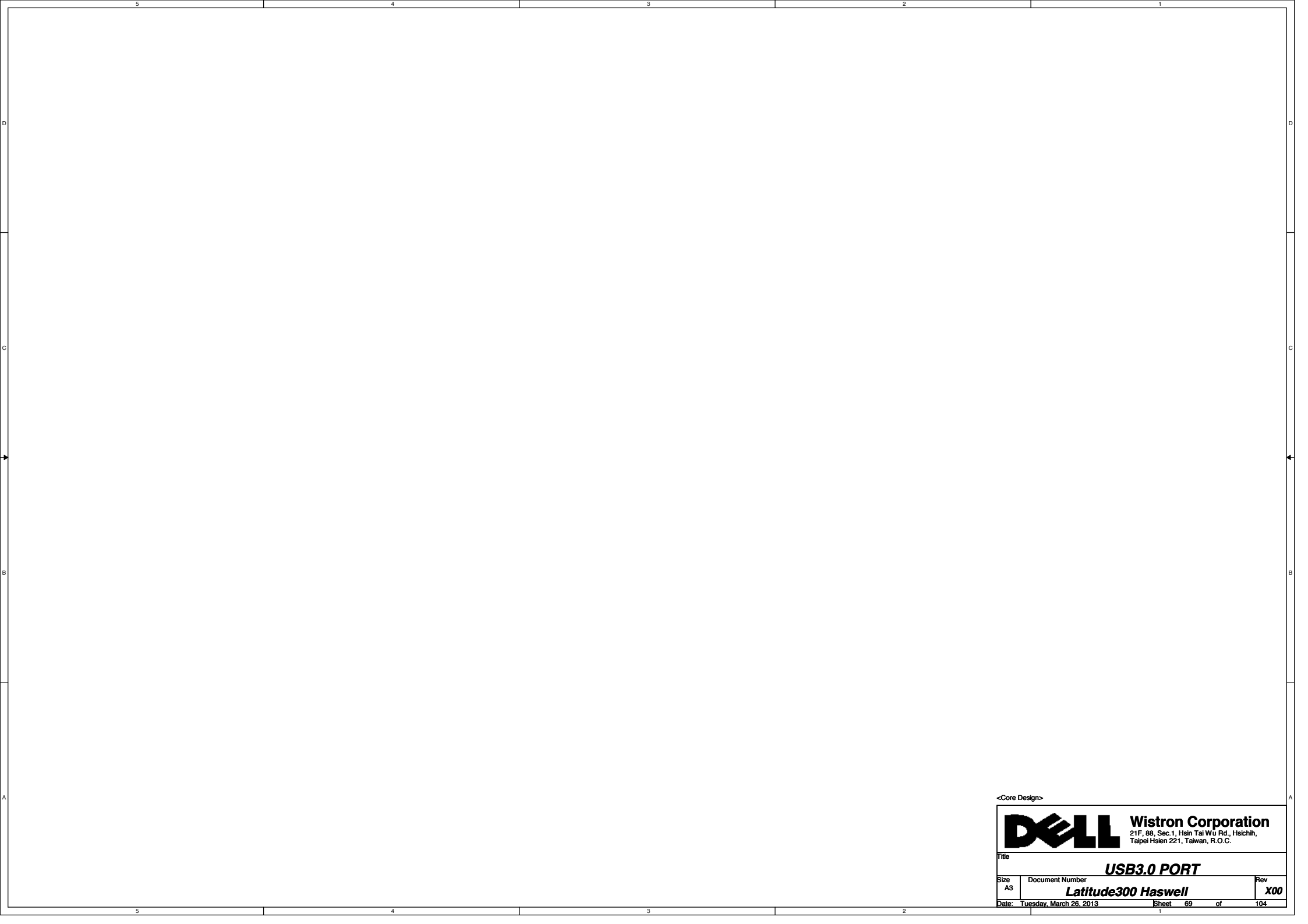
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title


**RESERVED**

|      |                            |            |
|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                 |
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| Date: Tuesday, March 26, 2013 | Sheet 68 of 104 |
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<Core Design>

|   |                            |  |            |
|---|----------------------------|--|------------|
|  |                            | <b>Wistron Corporation</b><br>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |            |
| Title   |                            |  |            |
| <b>USB3.0 PORT</b>  |                            |  |            |
| Size  | Document Number            |  | Rev        |
| A3  | <b>Latitude300 Haswell</b> |  | <b>X00</b> |
| Date:   | Tuesday, March 26, 2013    | Sheet  | 69 of 104  |

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title


***Reserved***

|      |                                   |                   |
|------|-----------------------------------|-------------------|
| Size | Document Number                   | Rev               |
| A3   | <b><i>Latitude300 Haswell</i></b> | <b><i>X00</i></b> |

|                               |                 |
|-------------------------------|-----------------|
| Date: Tuesday, March 26, 2013 | Sheet 70 of 104 |
|-------------------------------|-----------------|

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<Core Design>



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Title


**Reserved**

|      |                            |            |
|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                 |
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

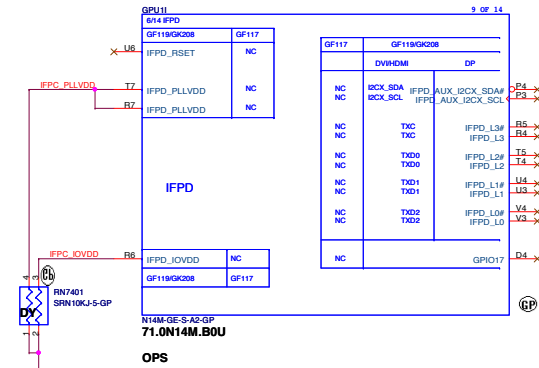
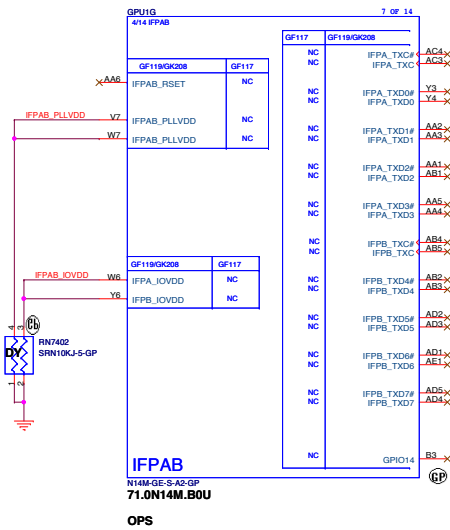
|      |                            |            |
|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                 |
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| Date: Tuesday, March 26, 2013 | Sheet 72 of 104 |
|-------------------------------|-----------------|

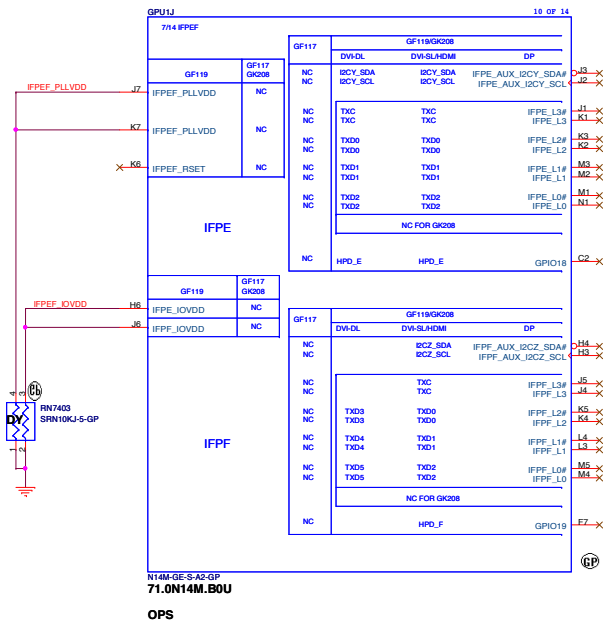
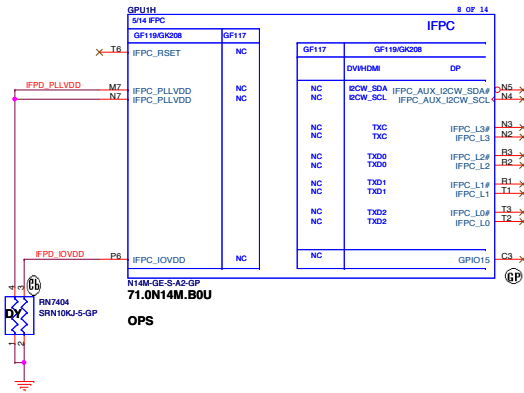


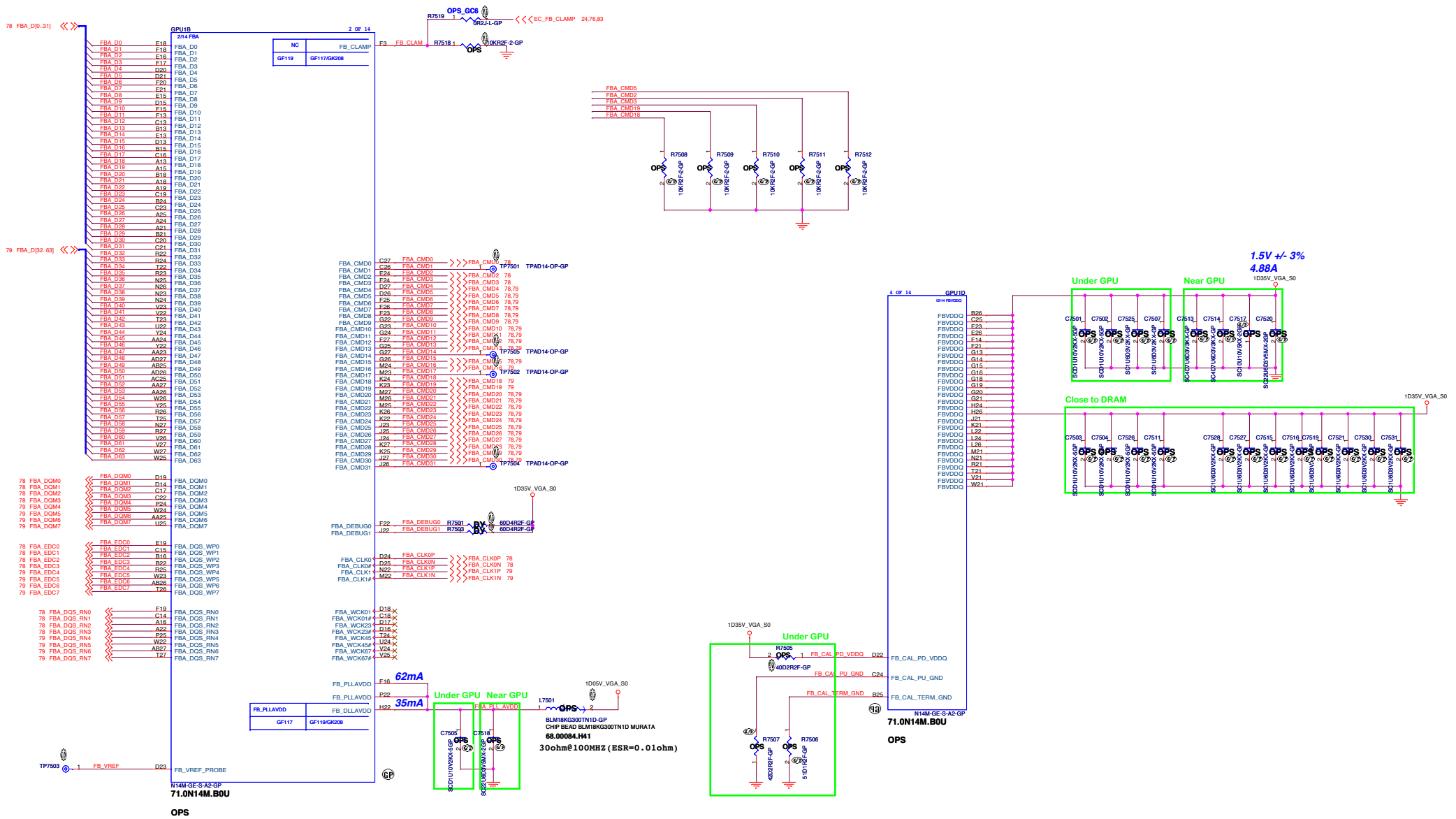


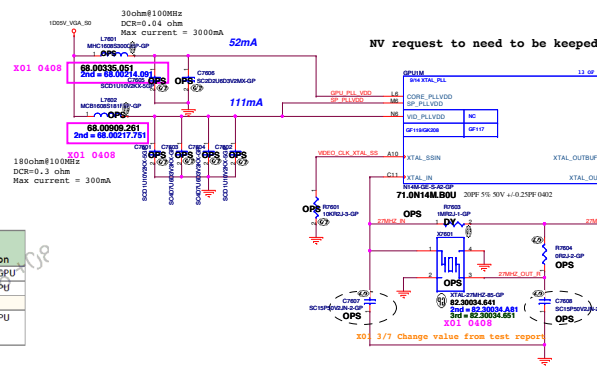
## LVDS Interface



## HDMI Interface

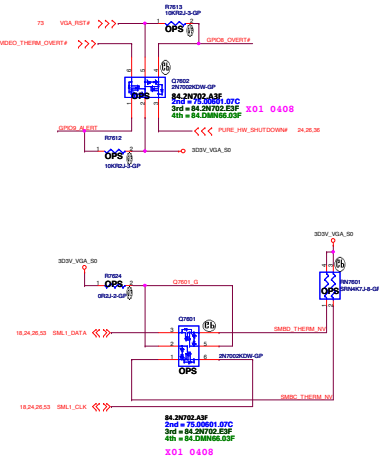






| GPU Package Type  | PLL Rail | Capacitor Type | Footprint | Population | Location  |
|---|----------|----------------|-----------|------------|-----------|
| G82-64 and G84-128                                      | PLL_VDD  | 100 nF         | X7R       | 0402       | Under GPU |
|   |          | 22 $\mu$ F     | X7R       | 0805       | 1         |
| <b>Bead Type</b>  |          |                |           |            |           |
| 30 $\Omega$ (ESR=0.010 for H4E-GE; 0.05 for all others) |          |                | 0402      | 1          | Heat GPU  |

| GPU Package Type            | PLL Rails                         | Capacitor Type                      | Footprint         | Population           | Location    |
|-----------------------------|-----------------------------------|-------------------------------------|-------------------|----------------------|-------------|
| GB2-64, GB4-128 and GB3-256 | SP_PLLVDD and VDD_PLLVDD combined | 100 nF<br>4.7 $\mu$ F<br>22 $\mu$ F | X7R<br>X5R<br>X5R | 0402<br>0402<br>0805 | 2<br>1<br>1 |
|                             |                                   | <b>Bead Type</b>                    |                   |                      |             |
|                             |                                   | 180 $\Omega$ (ESR=0.2)              | 0603              | 1                    | Heat GPU    |



| Configuration | Vendor  | Strap          | FBVDD/<br>FBVDDQ         | Manufacturer<br>Part Number | Max<br>Speed<br>CK<br>(MHz) | Memory<br>Date Code<br>Minimum | Status              |
|---------------|---------|----------------|--------------------------|-----------------------------|-----------------------------|--------------------------------|---------------------|
| 128M-16 DDR3  | Micron  | 0x1            | 1.5 V /<br>1.5 V         | MT41J128M16JT-<br>093G-K    | 1000                        | 1234                           | Production<br>ready |
|               |         |                | MT41J128M16JT-<br>107G-K | 900                         | 1150                        | Production<br>ready            |                     |
|               | Samsung | 0x5            | 1.5 V /<br>1.5 V         | K4W2G1646E-BC1A             | 1000                        | 1204                           | Production<br>ready |
|               |         |                | K4W2G1646E-BC11          | 900                         | 1204                        | Production<br>ready            |                     |
|               | Hynix   | 0x6            | 1.5V /<br>1.5V           | H5TQ2G63DFR-110C            | 1000                        | II/A                           | Production<br>ready |
|               |         |                | H5TQ2G63DFR-11C          | 900                         | II/A                        | Production<br>ready            |                     |
|               | 0xC     | 1.5V /<br>1.5V | H5TC2G63FFR-11C          | 1000                        | II/A                        | Post-production<br>candidate   |                     |

| Configuration | Vendor  | Strap | FBVDD/<br>FBVDDQ | Manufacturer<br>Part Number | Max<br>Speed<br>Kc<br>(MHz) | Memory<br>Data Code<br>Minimum | Status              |
|---------------|---------|-------|------------------|-----------------------------|-----------------------------|--------------------------------|---------------------|
| 256Mx16 DDR3  | Samsung | 0x3   | 1.5 V/<br>1.5 V  | K4W4G1646B-HC11             | 900                         | N/A                            | Production<br>ready |
|               | Micron  | 0x1   | 1.5 V/<br>1.5 V  | MT41K256M16HA-<br>107CE     | 900                         | N/A                            | Production<br>ready |
|               | Hynix   | 0x2   | 1.5V/<br>1.5V    | H5TC4G63A9R-11C             | 900                         | N/A                            | Production<br>ready |

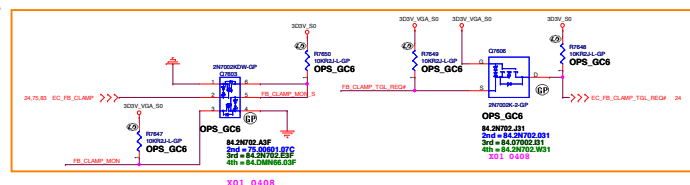
| Resistor Values | Pull-up to VDD33 | Pull-down to GND |
|-----------------|------------------|------------------|
| 4.99 k          | 1000             | 0000             |
| 10.0 k          | 1001             | 0001             |
| 15.0 k          | 1010             | 0010             |
| 20.0 k          | 1011             | 0011             |
| 24.9 k          | 1100             | 0100             |
| 30.1 k          | 1101             | 0101             |
| 34.8 k          | 1110             | 0110             |
| 45.3 k          | 1111             | 0111             |

| Strap Pin Name | Strap Mapping  | Resistance | Polarity  |
|----------------|----------------|------------|---|
| ROM_SCLX       | SUB_ALT_ADDR   | 10k Ω      | Pull-down to GND  |
| ROM_SI         | SUB_VEHOR      | 10k Ω      | Pull-up to 3V3 if YBIOS ROM exists,<br>Pull-down to GND if no YBIOS ROM |
| ROM_S0         | VGA_DEVICE     | 10k Ω      | Pull-down to GND (no display)   |
| STRAP0         | RAM_CFG[0]     | 10k Ω      | See Note below  |
| STRAP1         | RAM_CFG[1]     | 10k Ω      | See Note below  |
| STRAP2         | RAM_CFG[2]     | 10k Ω      | See Note below  |
| STRAP3         | RAM_CFG[3]     | 10k Ω      | See Note below  |
| STRAP4         | PCIE_MAX_SPEED | 10k Ω      | Pull-down to GND  |

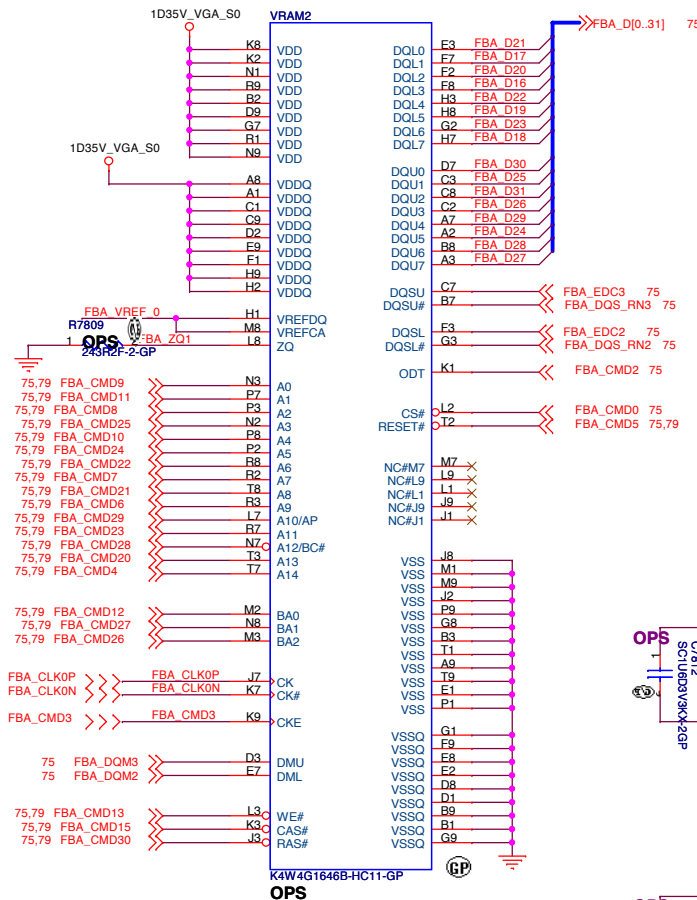
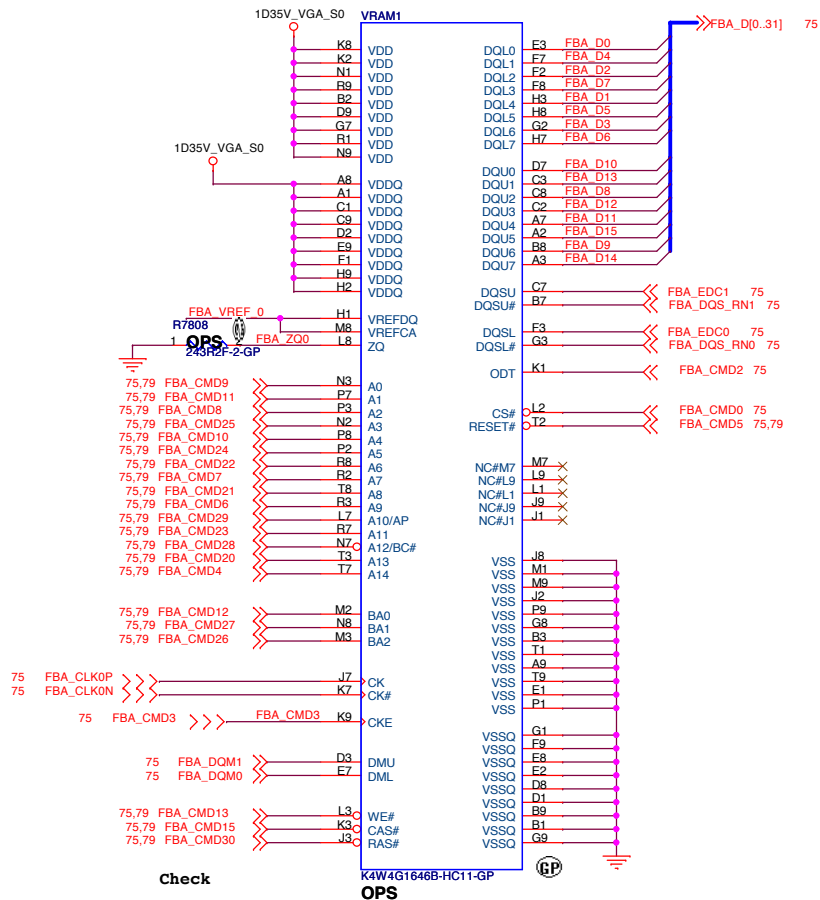
|             | N14M-LP                      | N14M-GS                      | N14P-GV                      | N14P-GV2                     |
|-------------|------------------------------|------------------------------|------------------------------|------------------------------|
| Chip Part # | GK208-640<br>(Small package) | GK208-630<br>(Small package) | GK208-650<br>(Small package) | GK208-632<br>(Small package) |
|             | GK208-740<br>(Big package)   | GK208-730<br>(Big package)   | GK208-750<br>(Big package)   | GK208-732<br>(Big package)   |
| Device ID   | 0x1291                       | 0x1290                       | 0x1294                       | 0x1292                       |

[illegible]

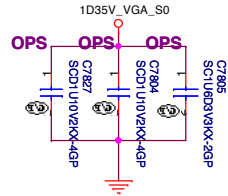
|  | N14M-GE/G-L | Other N14x GPUs       |
|--|-------------|-----------------------|
| Multi_Strap_Ref2_GND<br>(Only on G82-44 package) | No Connect  | N/A                   |
| Multi_Strap_Ref1_GND<br>(Only on G82-44 package) | No Connect  | N/A                   |
| Multi_Strap_Ref0_GND                             | No Connect  | 40.2k $\Omega$ to GND |
| Strap Mode Selected                              | Binary      | Multi-Level           |



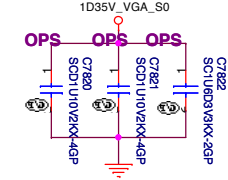




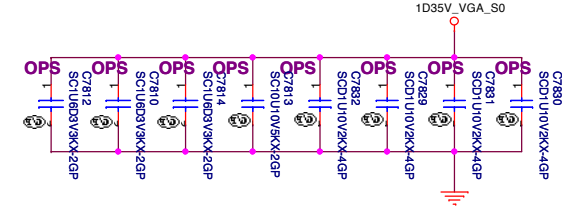
Place close VRAM1 VDD ball



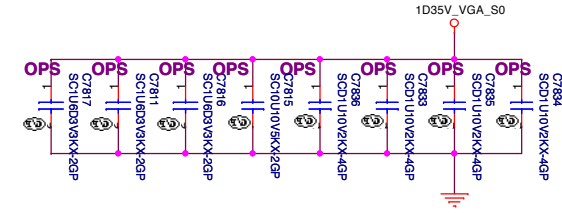
Place close VRAM2 VDD ball



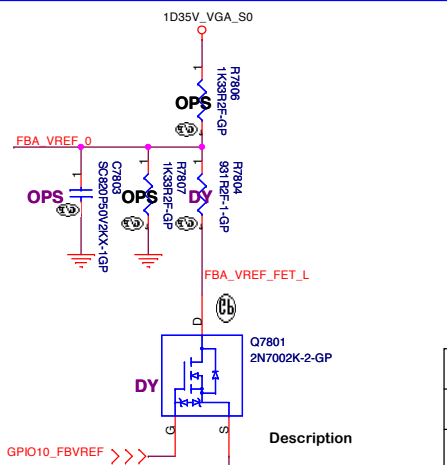
Place close VRAM1VDDQ ball



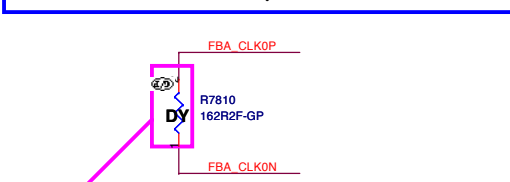
Place close VRAM1VDDQ ball



## Frame Buffer Partition A-Lower Half



## FBCLK Termination place on VRAM side



X01 stuff R7802 R7801 C7801,DY R7810 for CLK reference 0411

## FBVREF Termination

| Type           | FBVREF% | Voltage | GPU_GPIO10 |
|----------------|---------|---------|------------|
| Un-termination | 50%     | 0.749V  | High       |
| Termination    | 70%     | 1.0617V | Low        |

Description

84.2N702.331  
2nd = 84.2N702.031  
3rd = 84.07002.131  
4th = 84.2N702.W31

X01 0408

20110613

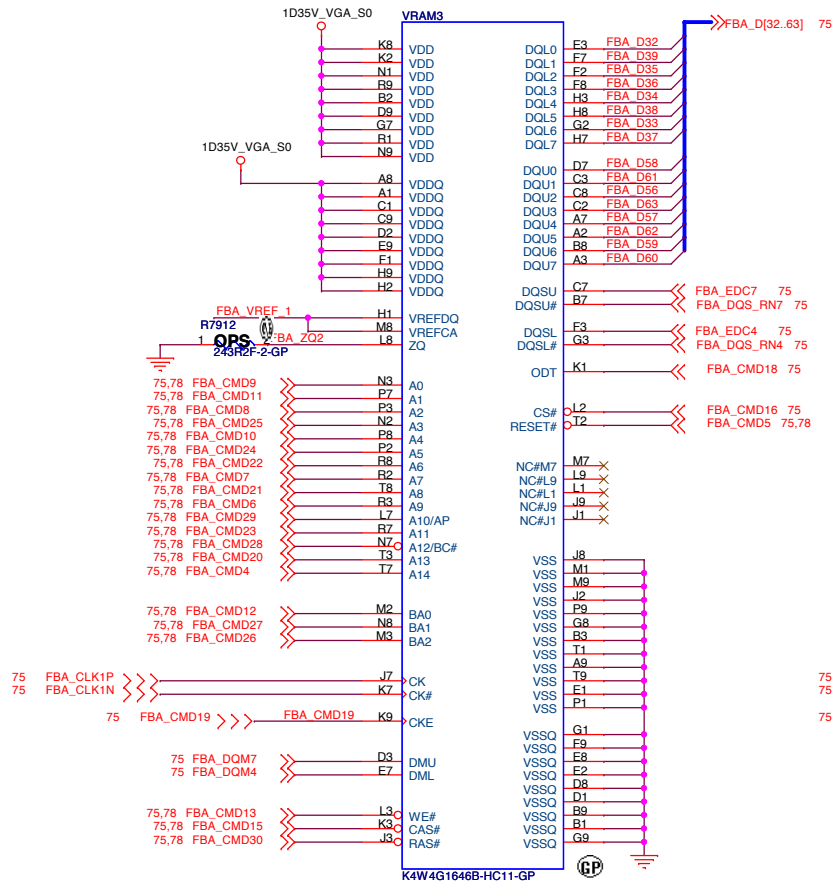
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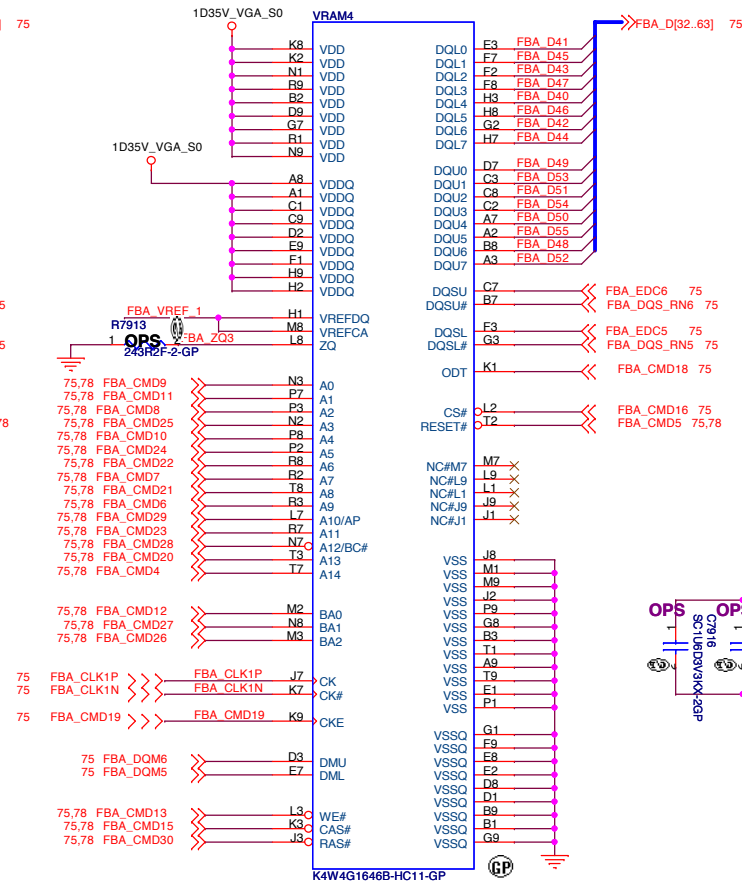
Title: **GPU-VRAM1,2 (1/4)**

Size A3 Document Number: **Latitude300 Haswell** Rev **X00**

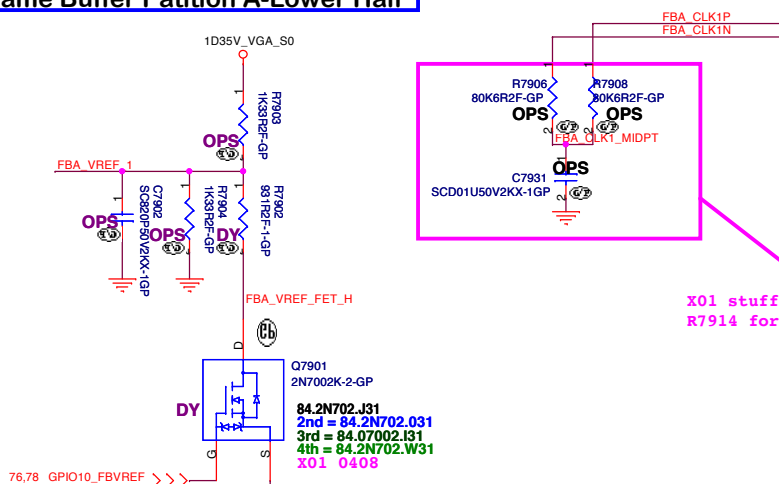
Date: Friday, April 19, 2013 Sheet 78 of 104



Frame Buffer Partition A-Lower Half

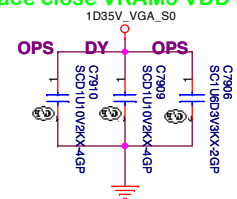


FBCLK Termination place on VRAM side

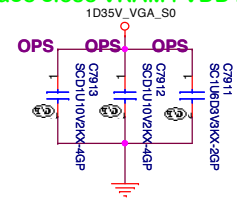


X01 stuff R7906 R7908 C7931,DY  
R7914 for CLK reference 0411

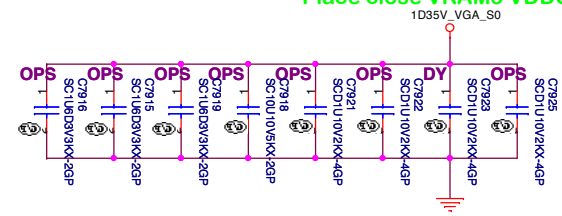
Place close VRAM3 VDD ball



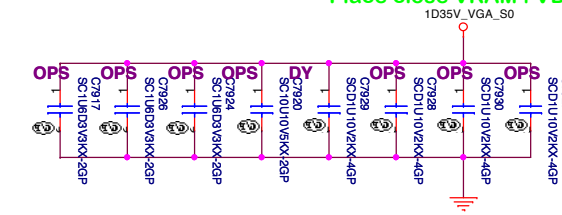
Place close VRAM4 VDD ball



Place close VRAM3 VDDQ ball

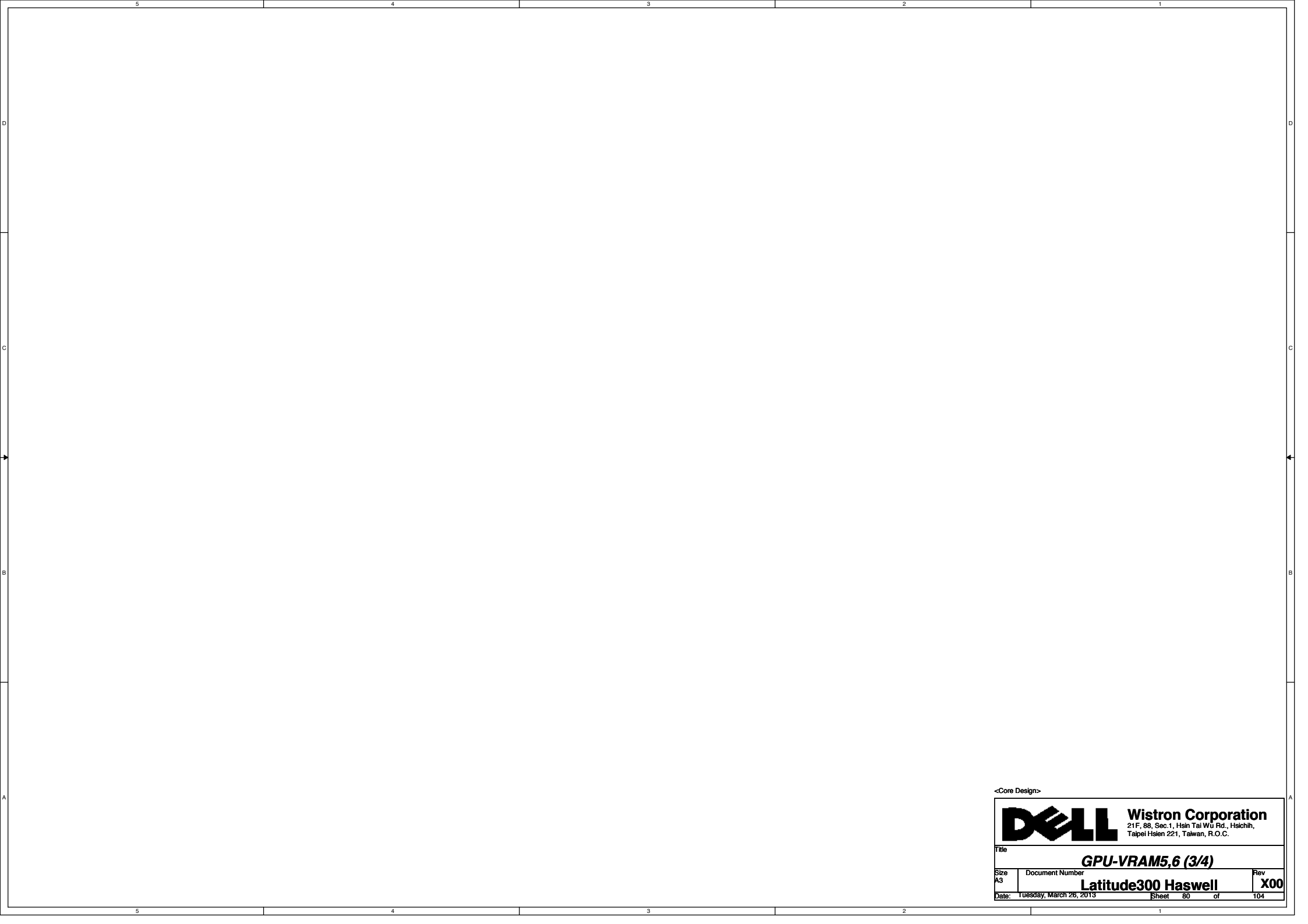


Place close VRAM4 VDDQ ball



<Core Design>

|                              |                  |   |  |
|------------------------------|------------------|---|--|
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|                              |                  | Title: <b>GPU-VRAM3,4 (2/4)</b>   |  |
| Size: A3                     | Document Number: | Rev: X00  |  |
| Date: Friday, April 19, 2013 | Sheet: 79        | of 104  |  |



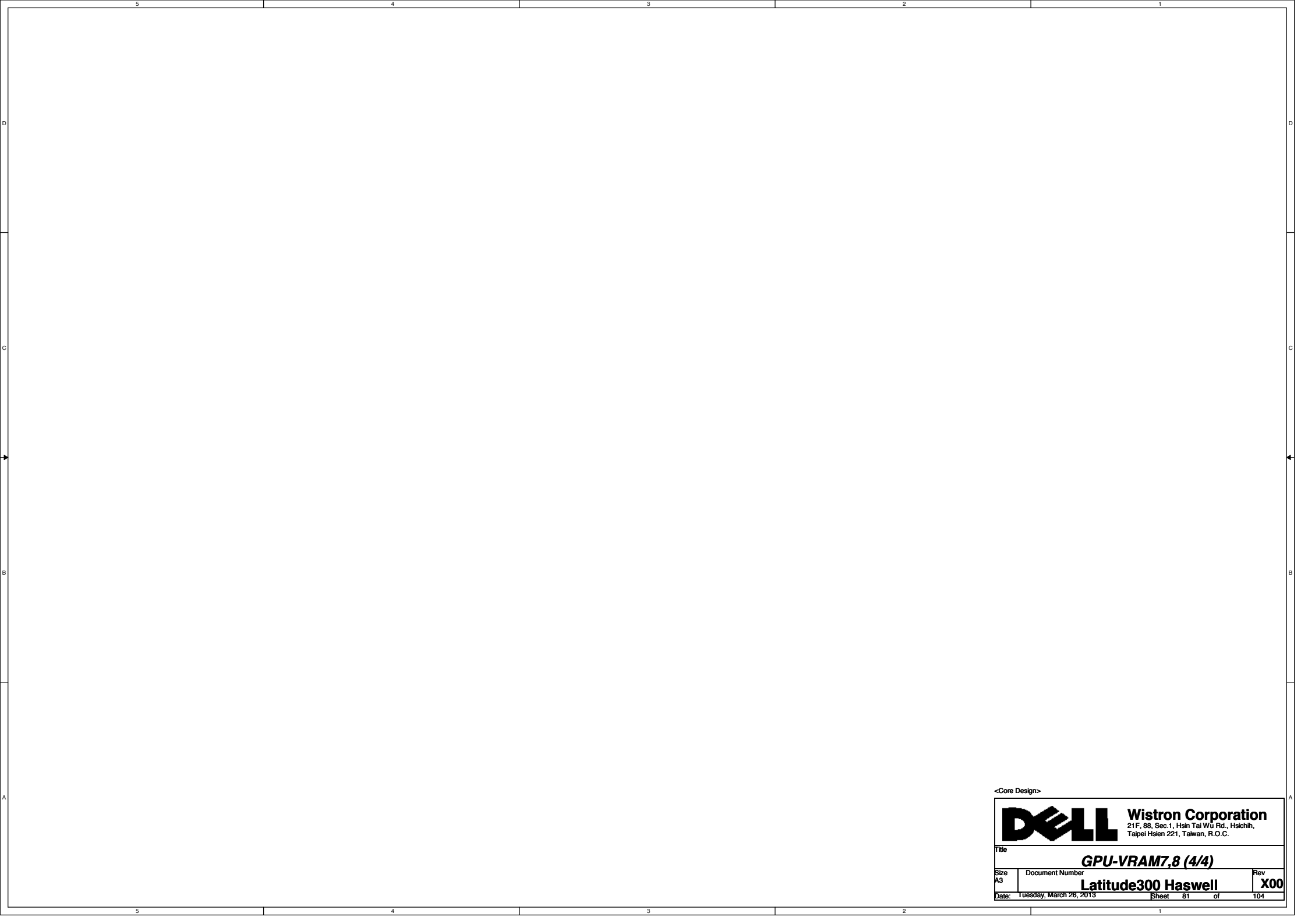
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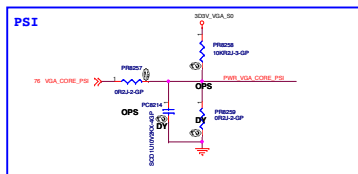
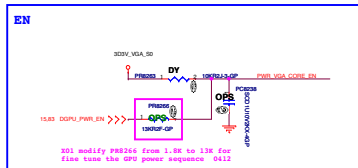
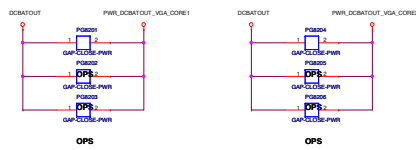
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|-------------------|-------------------------|-----------------|
| Title             |                         |                 |
| GPU-VRAM5,6 (3/4) |                         |                 |
| Size              | Document Number         | Rev             |
| A3                | Latitude300 Haswell     | X00             |
| Date:             | Tuesday, March 26, 2013 | Sheet 80 of 104 |



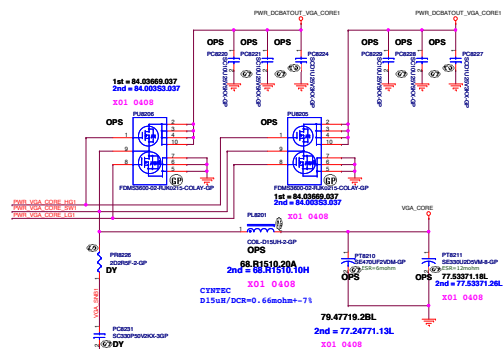


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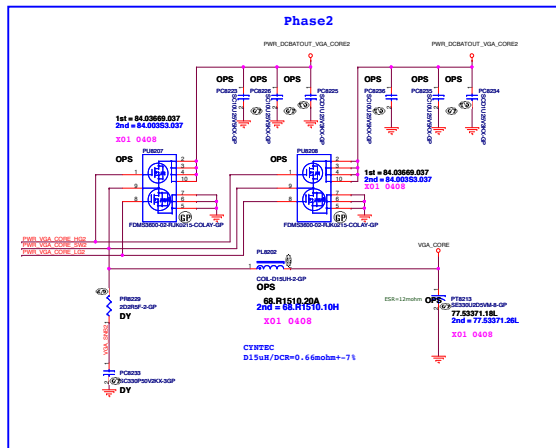
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|---|----------------------------|---|-----------------|
|  |                            | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                 |
| Title   |                            |   |                 |
| <b>GPU-VRAM7,8 (4/4)</b>  |                            |   |                 |
| Size  | Document Number            |   | Rev             |
| A3  | <b>Latitude300 Haswell</b> |   | <b>X00</b>      |
| Date:   | Tuesday, March 26, 2013    |   | Sheet 81 of 104 |



### Phase1

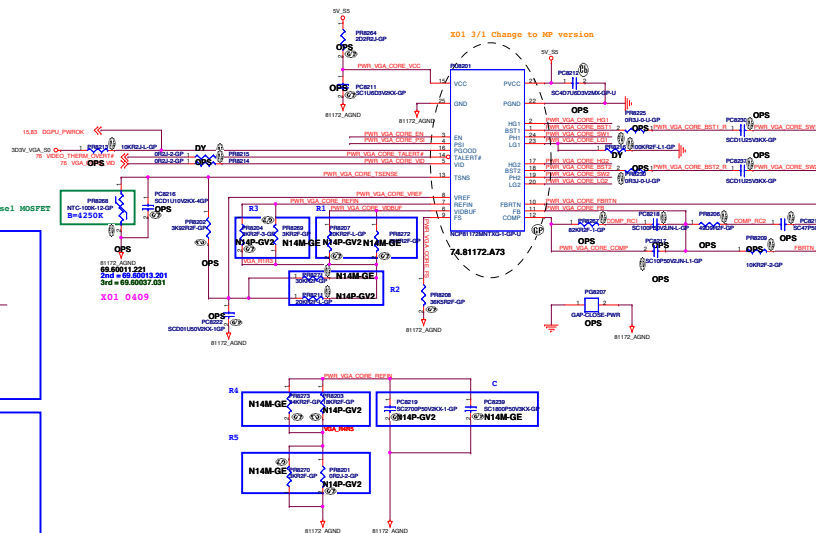


I/P caps: 100 25V X805 X56/ 78.10622.51L  
 MOS: Q1: Id=10A, Rds(on)=9.8-13.2 mohm ; Q2: Id=17A, Rds(on)=3.6-5.2mohm 84.03669.037  
 Inductors: CHIP CHOKER 0.22uH PCB0637-822M5 2.5-3mohm 1sat =34Arms 68.82210.20C  
 O/P caps: CHIP CAP POL 3300 2.5V H 6.3\*4.5 2.3Arms Matsuti/77.53371.18L



I/P caps: 100 25V X805 X56/ 78.10622.51L  
 MOS: Q1: Id=10A, Rds(on)=9.8-13.2 mohm ; Q2: Id=17A, Rds(on)=3.6-5.2mohm 84.03669.037  
 Inductors: CHIP CHOKER 0.22uH PCB0637-822M5 2.5-3mohm 1sat =34Arms 68.82210.20C  
 O/P caps: CHIP CAP POL 3300 2.5V H 6.3\*4.5 2.3Arms Matsuti/77.53371.18L

### X01 3/1 Change to HP version



2012-12-06 (Power team modify)  
 PWR228 and PWR227 change to  
 100R(54.10005.000) 5V15kA Suggess

### EDC=45A EDP=72A

| TYPE     | config | TDC | SDP | ODP | R1/PWR207 | R2/PWR211 | R3/PWR204 | R4/PWR203 | R5/PWR201 | C/PCB219 |
|----------|--------|-----|-----|-----|-----------|-----------|-----------|-----------|-----------|----------|
| N14M-GE  | C      | 35A | 41A |     | 39kohm    | 30kohm    | 3kohm     | 24kohm    | 3kohm     | 1.8nF    |
| N14P-GV2 | B      | 32A | 55A |     | 20kohm    | 20kohm    | 2kohm     | 18kohm    | 0ohm      | 2.7nF    |
| N14P-GT  | B      | 45A | 75A |     | 20kohm    | 20kohm    | 2kohm     | 18kohm    | 0ohm      | 2.7nF    |

Table 1. PWM-VID Spec and Component Values

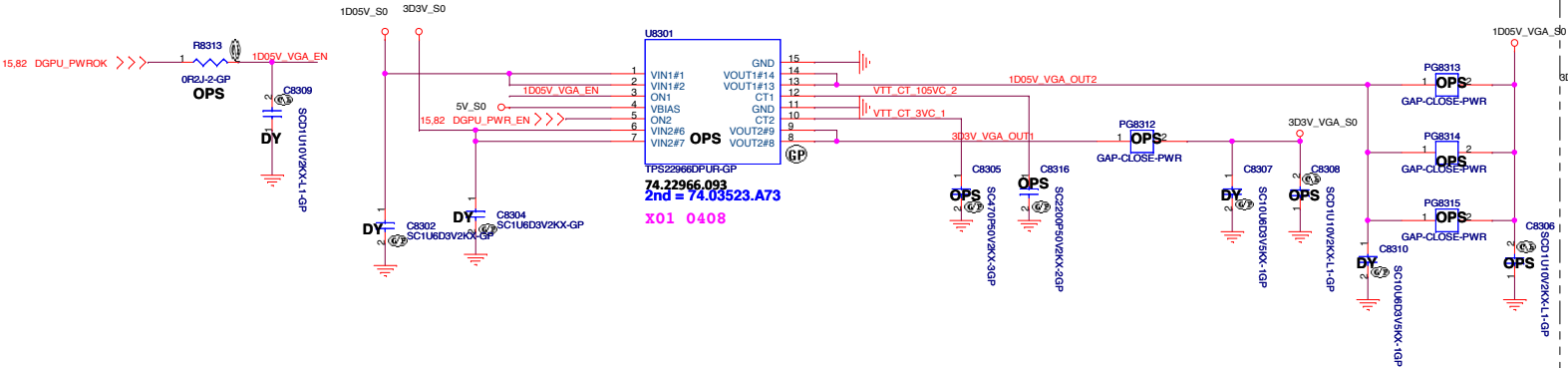
| PWM-VID Spec                            | Config A  | Config B | Config C |
|---|-----------|----------|----------|
| Vmin                                    | 0.6       | 0.6      | 0.65     |
| Vmax                                    | 1.2       | 1.2      | 1.15     |
| Vboot                                   | 0.875     | 0.9      | 0.9      |
| Voltage Step Vstep                      | mV 6.25   | 6.25     | 3.5      |
| Number of Voltage Levels N              | level 96  | 96       | 20       |
| PWM Frequency F <sub>SW</sub>           | MHz 1.125 | 1.125    | 0.676    |
| PWM Minimum Pulse Width T <sub>ON</sub> | ns 9.26   | 9.26     | 74       |
| VID Transient Time T                    | us <100   | <100     | <100     |
| Component Value                         |           |          |          |
| R1 (1%)                                 | KΩ 39     | 20       | 39       |
| R2 (1%)                                 | KΩ 39     | 20       | 30       |
| R3 (1%)                                 | KΩ 1.5    | 2        | 3        |
| R4 (1%)                                 | KΩ 30     | 18       | 24       |
| R5 (1%)                                 | KΩ 1.5    | 0        | 3        |
| C                                       | nF 1.5    | 2.7      | 1.8      |

<Core Design>

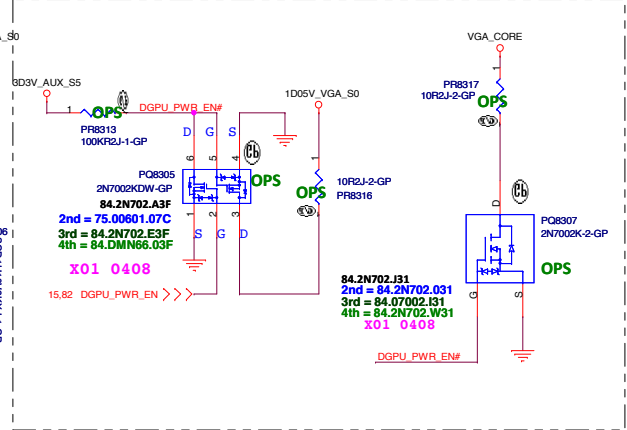
3D3V\_VGA\_S0  
1D05V\_VGA\_S0

3D3V\_VGA\_S0 should ramp-up before VGA\_Core  
VGA\_Core should ramp-up before 1D05V\_VGA\_S0  
1D35V\_VGA\_S0 should ramp-up before 1D05V\_VGA\_S0

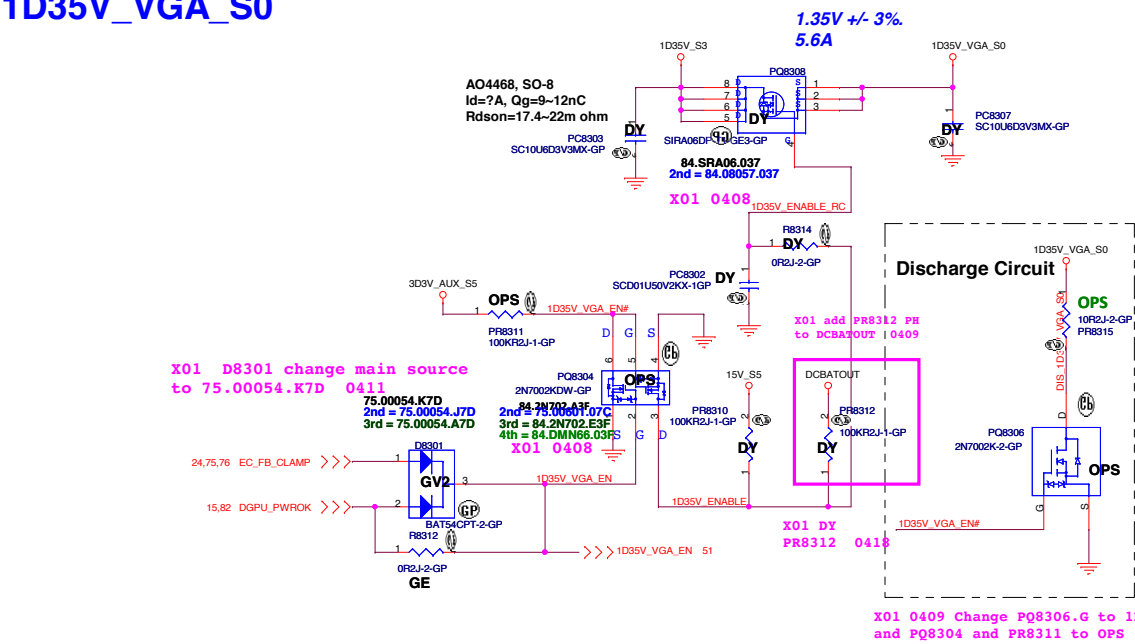
3D3V\_S0 to 3D3V\_VGA\_S0  
1D05V\_S0 to 1D05V\_VGA\_S0



0307 Add Discharge Circuit



1D35V\_VGA\_S0



| C <sub>Tx</sub> (pF) | Rise Time (μs) 10% - 90%, C <sub>OUT</sub> = 0.1μF @ V <sub>IN</sub> ; V <sub>OUT</sub> =0 ohm load |       |      |      |      |       |      |      |
|----------------------|---|-------|------|------|------|-------|------|------|
|                      | Typical values @ 25°C, 25V X7R 10% ceramic cap  |       |      |      |      |       |      |      |
|                      | 5V  | 3.3V  | 1.8V | 1.5V | 1.2V | 1.05V | 1V   | 0.8V |
| 0                    | 107   | 72    | 46   | 41   | 36   | 34    | 33   | 29   |
| 220                  | 425   | 276   | 146  | 122  | 103  | 91    | 88   | 74   |
| 270                  | 489   | 316   | 172  | 139  | 121  | 107   | 104  | 84   |
| 470                  | 774   | 487   | 272  | 224  | 181  | 159   | 154  | 123  |
| 680                  | 1108  | 708   | 375  | 317  | 242  | 221   | 213  | 168  |
| 1000                 | 1561  | 1007  | 546  | 441  | 364  | 314   | 299  | 234  |
| 2200                 | 3600  | 2289  | 1240 | 1019 | 817  | 681   | 665  | 539  |
| 4700                 | 7757  | 5092  | 2674 | 2203 | 1808 | 1592  | 1516 | 1177 |
| 10000                | 15700   | 10310 | 5601 | 4659 | 3674 | 3401  | 3197 | 2562 |

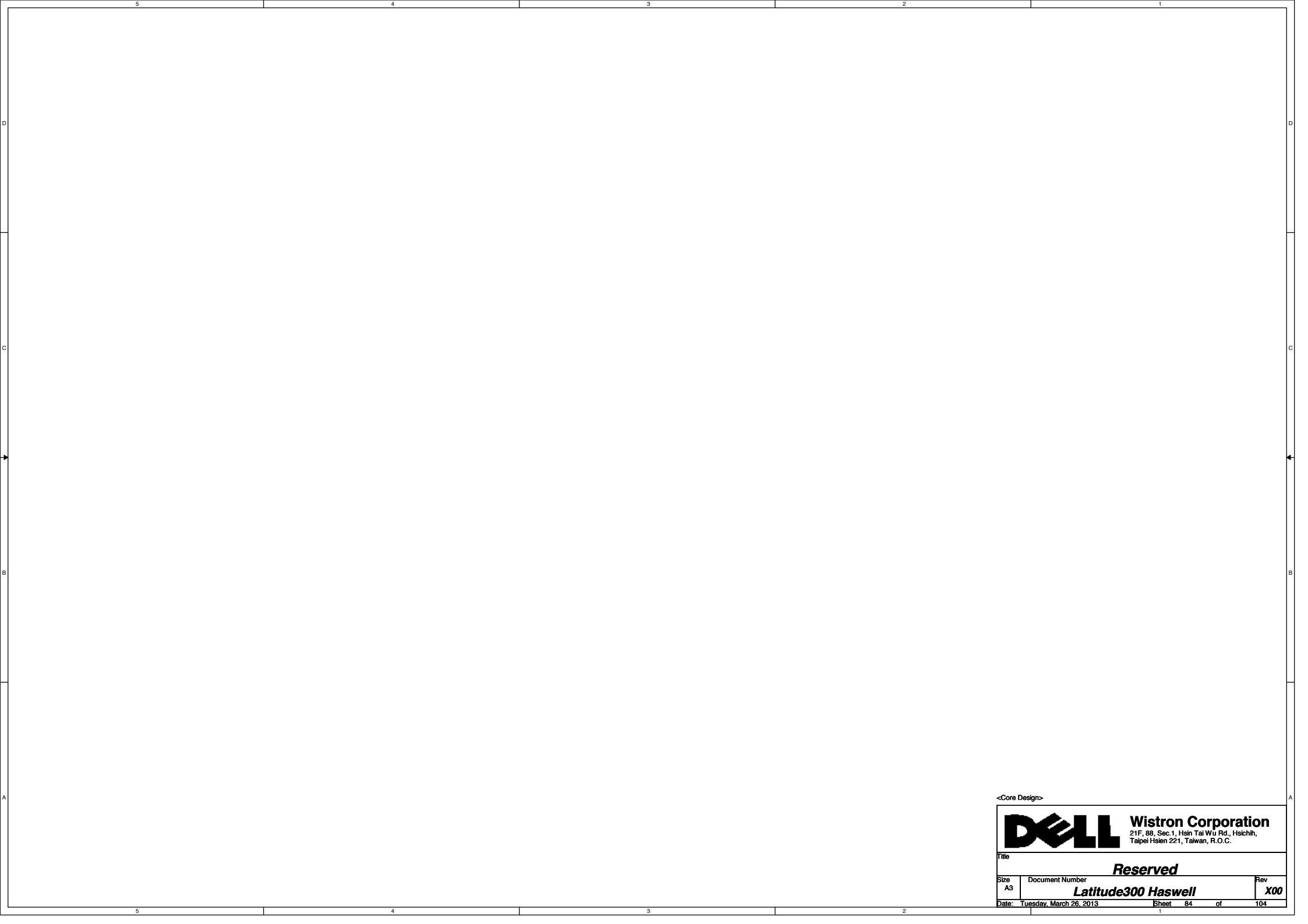
Table 1. Rise time vs. C<sub>Tx</sub> value

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Title **DISCRETE VGA POWER**

|                              |                            |            |
|------------------------------|----------------------------|------------|
| Size                         | Document Number            | Rev        |
| Custom                       | <b>Latitude300 Haswell</b> | <b>X00</b> |
| Date: Friday, April 19, 2013 | Sheet 83 of                | 104        |




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|   |  |  |                          |
|---|--|--|--------------------------|
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| Title   |  |  |                          |
| <b><i>Reserved</i></b>  |  |  |                          |
| Size<br>A3  | Document Number<br><b><i>Latitude300 Haswell</i></b> |  | Rev<br><b><i>X00</i></b> |
| Date: Tuesday, March 26, 2013   | Sheet  | 84   | of 104                   |

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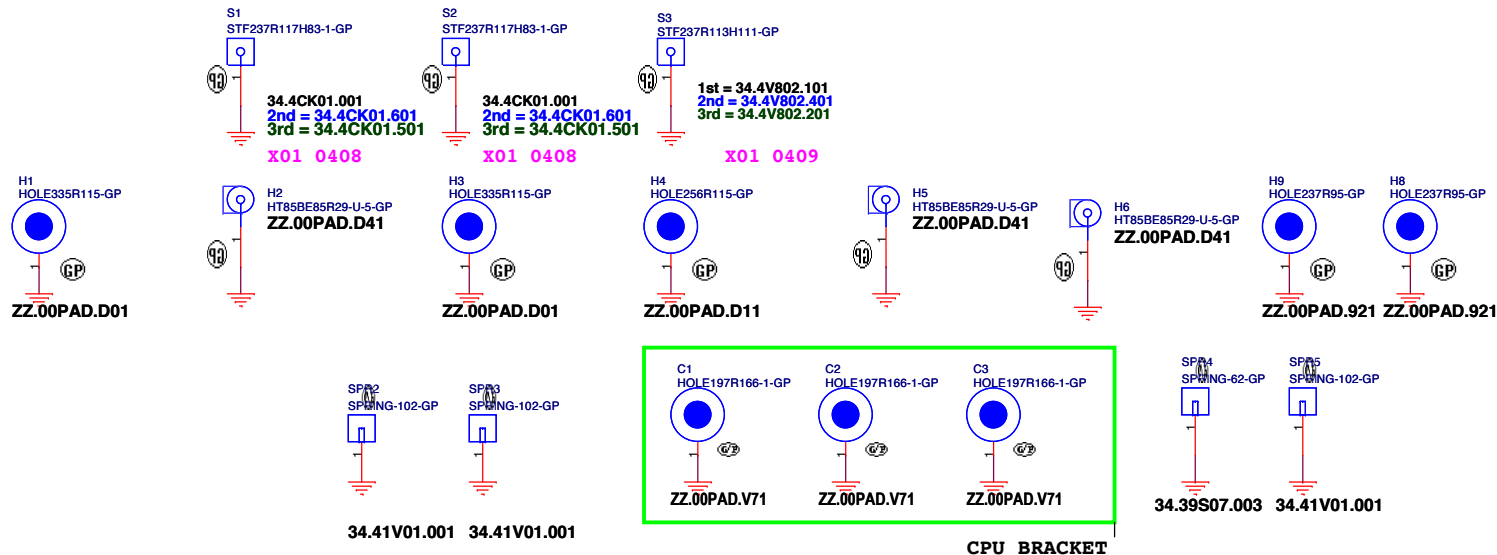
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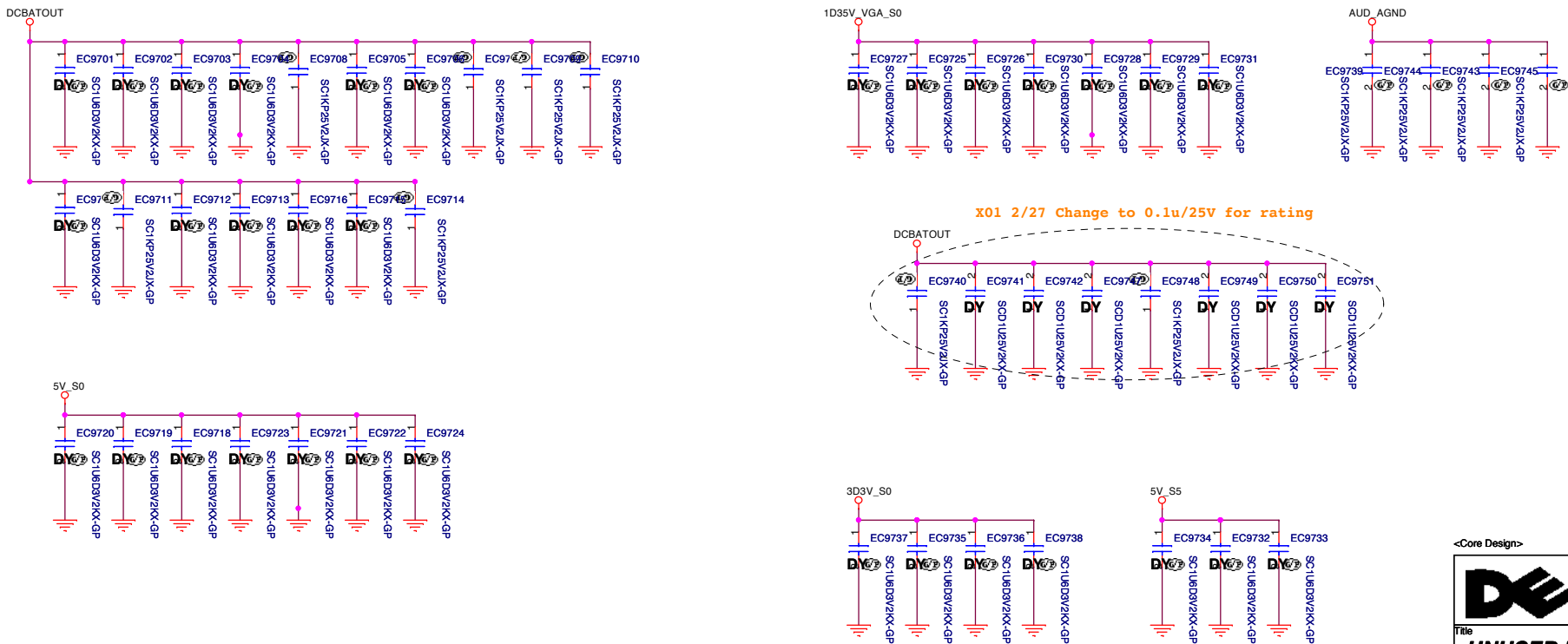
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|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                 |
|-------------------------------|-----------------|
| Date: Tuesday, March 26, 2013 | Sheet 85 of 104 |
|-------------------------------|-----------------|

# SSID = Mechanical




# SSID = EMI



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Title


**Reserved**

|      |                            |            |
|------|----------------------------|------------|
| Size | Document Number            | Rev        |
| A3   | <b>Latitude300 Haswell</b> | <b>X00</b> |

|                               |                 |
|-------------------------------|-----------------|
| Date: Tuesday, March 26, 2013 | Sheet 87 of 104 |
|-------------------------------|-----------------|

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Title

**Reserved**


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**Free Fall Sensor**

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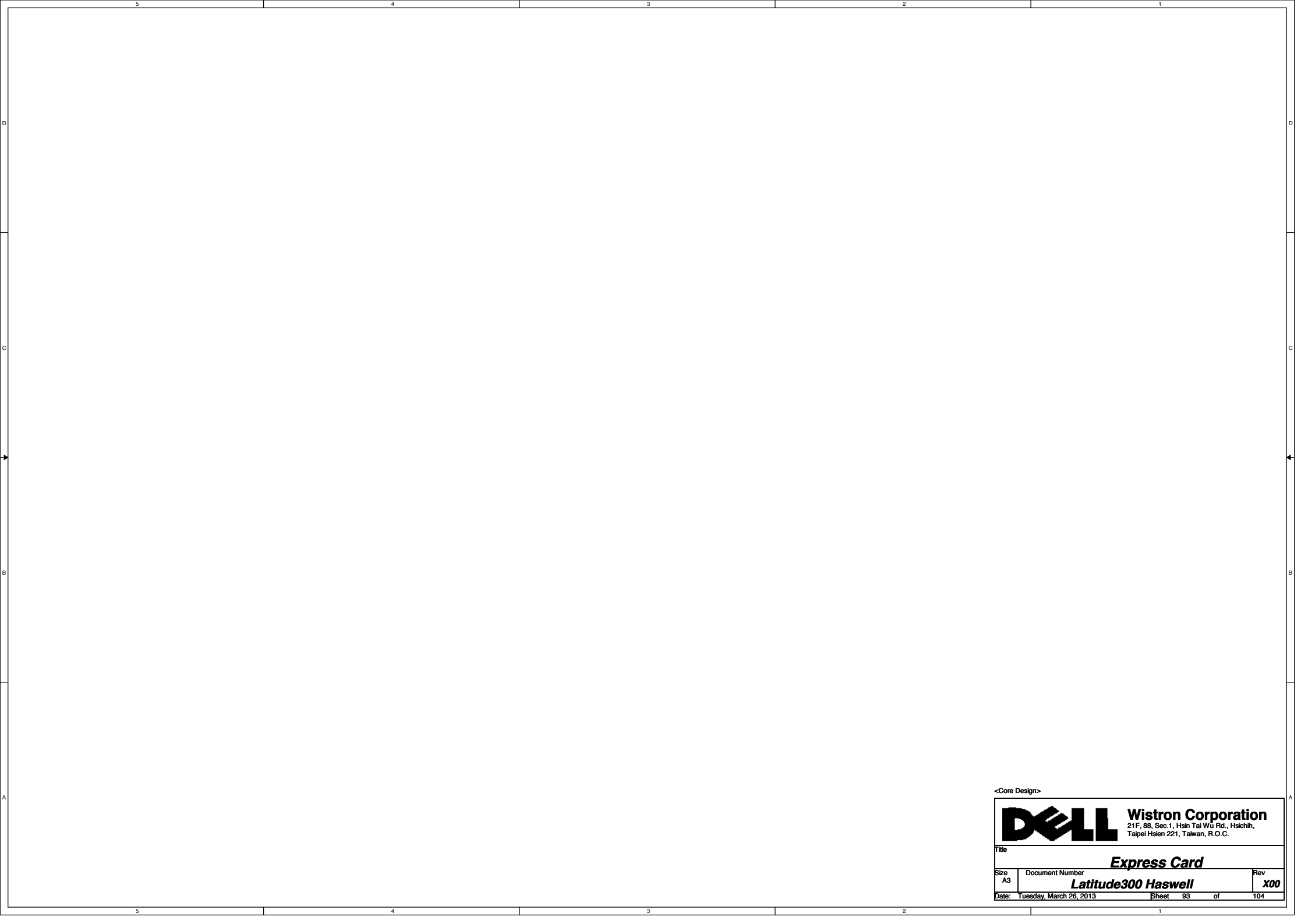
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| Title |                            |       | <b>Express Card</b> |            |
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**LVDS Switch**

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Title

CRT Switch

Size

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Document Number

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Rev

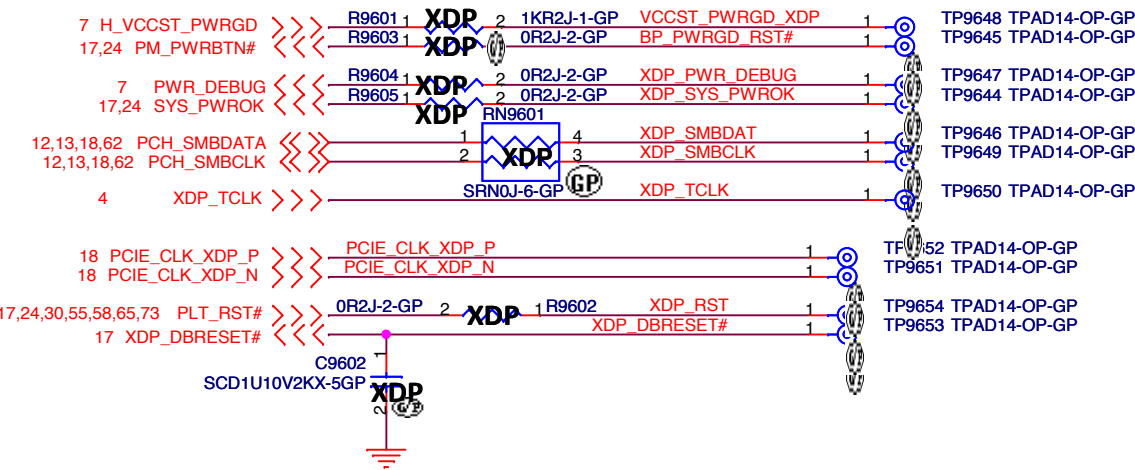
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SSID = XDP

CPU XDP



- TP9601 TPAD14-OP-GP
- TP9602 TPAD14-OP-GP
- TP9624 TPAD14-OP-GP
- TP9621 TPAD14-OP-GP
- TP9623 TPAD14-OP-GP
- TP9611 TPAD14-OP-GP
- TP9612 TPAD14-OP-GP
- TP9613 TPAD14-OP-GP
- TP9614 TPAD14-OP-GP
- TP9615 TPAD14-OP-GP
- TP9616 TPAD14-OP-GP
- TP9617 TPAD14-OP-GP
- TP9618 TPAD14-OP-GP
- TP9619 TPAD14-OP-GP
- TP9626 TPAD14-OP-GP
- TP9627 TPAD14-OP-GP
- TP9620 TPAD14-OP-GP
- TP9622 TPAD14-OP-GP
- TP9630 TPAD14-OP-GP
- TP9631 TPAD14-OP-GP
- TP9629 TPAD14-OP-GP
- TP9628 TPAD14-OP-GP
- TP9634 TPAD14-OP-GP
- TP9635 TPAD14-OP-GP
- TP9633 TPAD14-OP-GP
- TP9632 TPAD14-OP-GP
- TP9637 TPAD14-OP-GP
- TP9639 TPAD14-OP-GP
- TP9638 TPAD14-OP-GP
- TP9636 TPAD14-OP-GP
- TP9640 TPAD14-OP-GP
- TP9643 TPAD14-OP-GP
- TP9642 TPAD14-OP-GP
- TP9641 TPAD14-OP-GP

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**TOUCH PANEL**

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**Latitude300 Haswell**

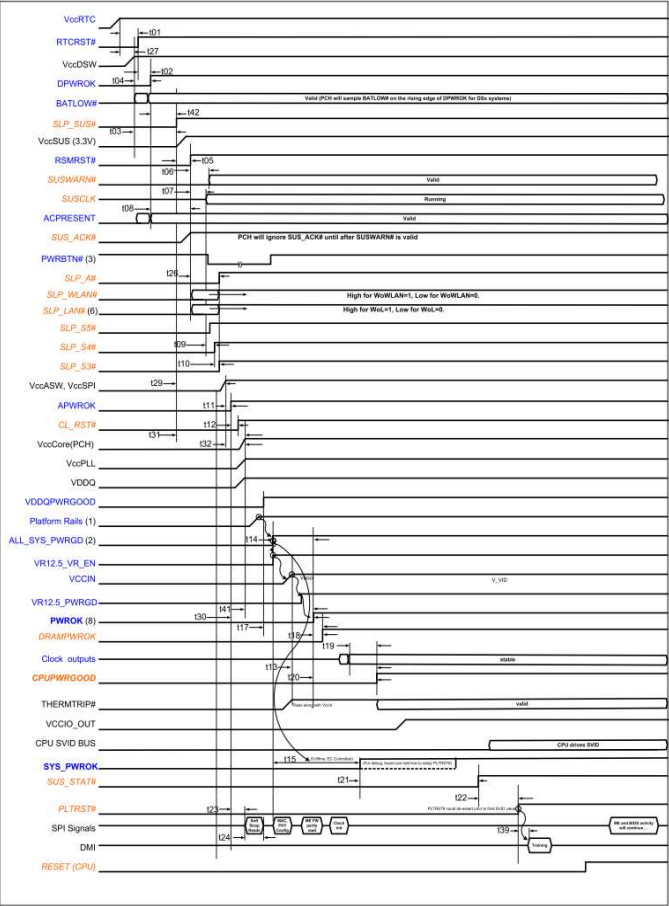
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**X00**

Date: Friday, April 19, 2013

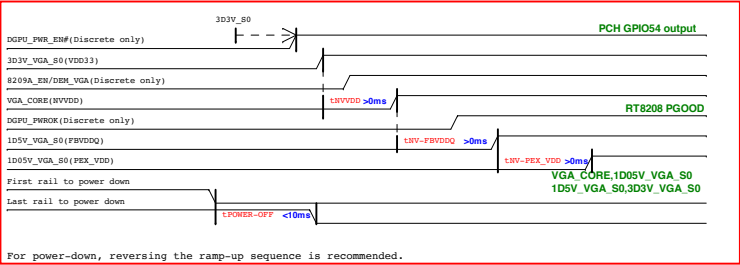
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Shark Bay Platform Power Sequence

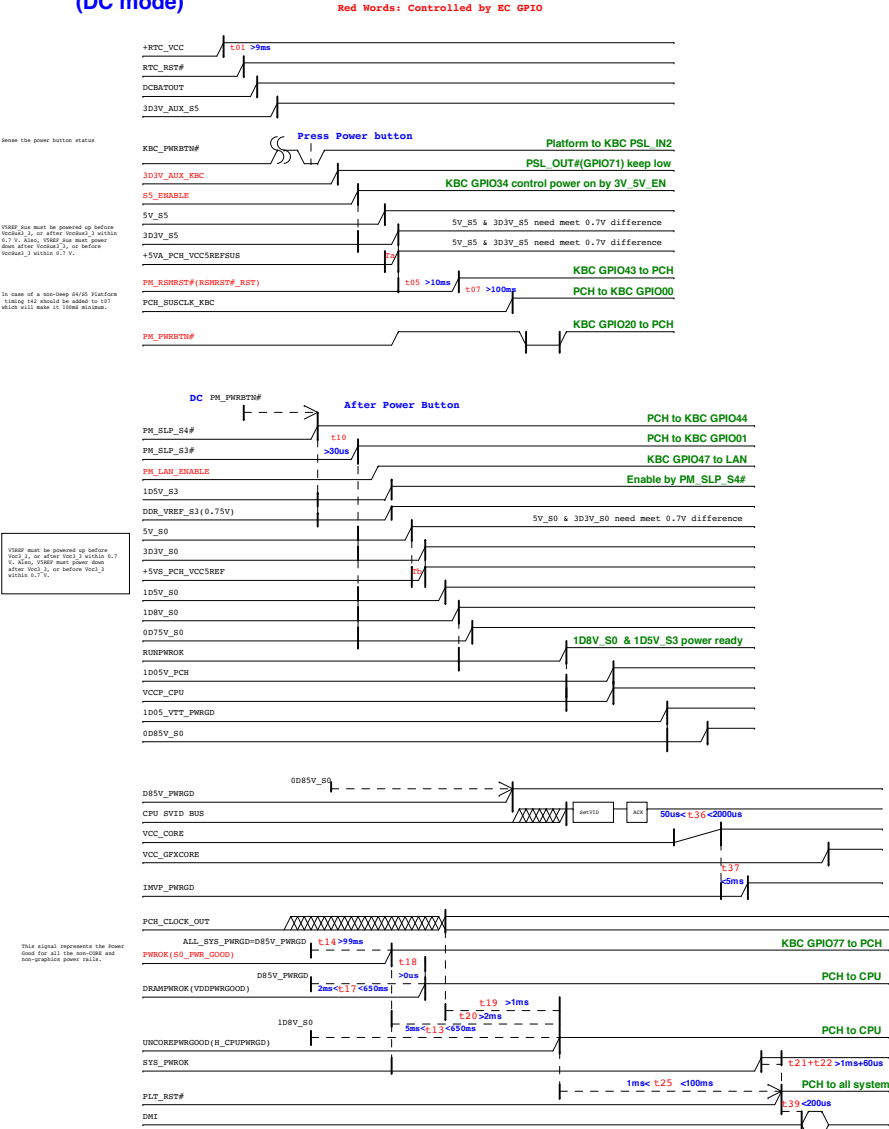


N14P-GT Power-Up/Down Sequence

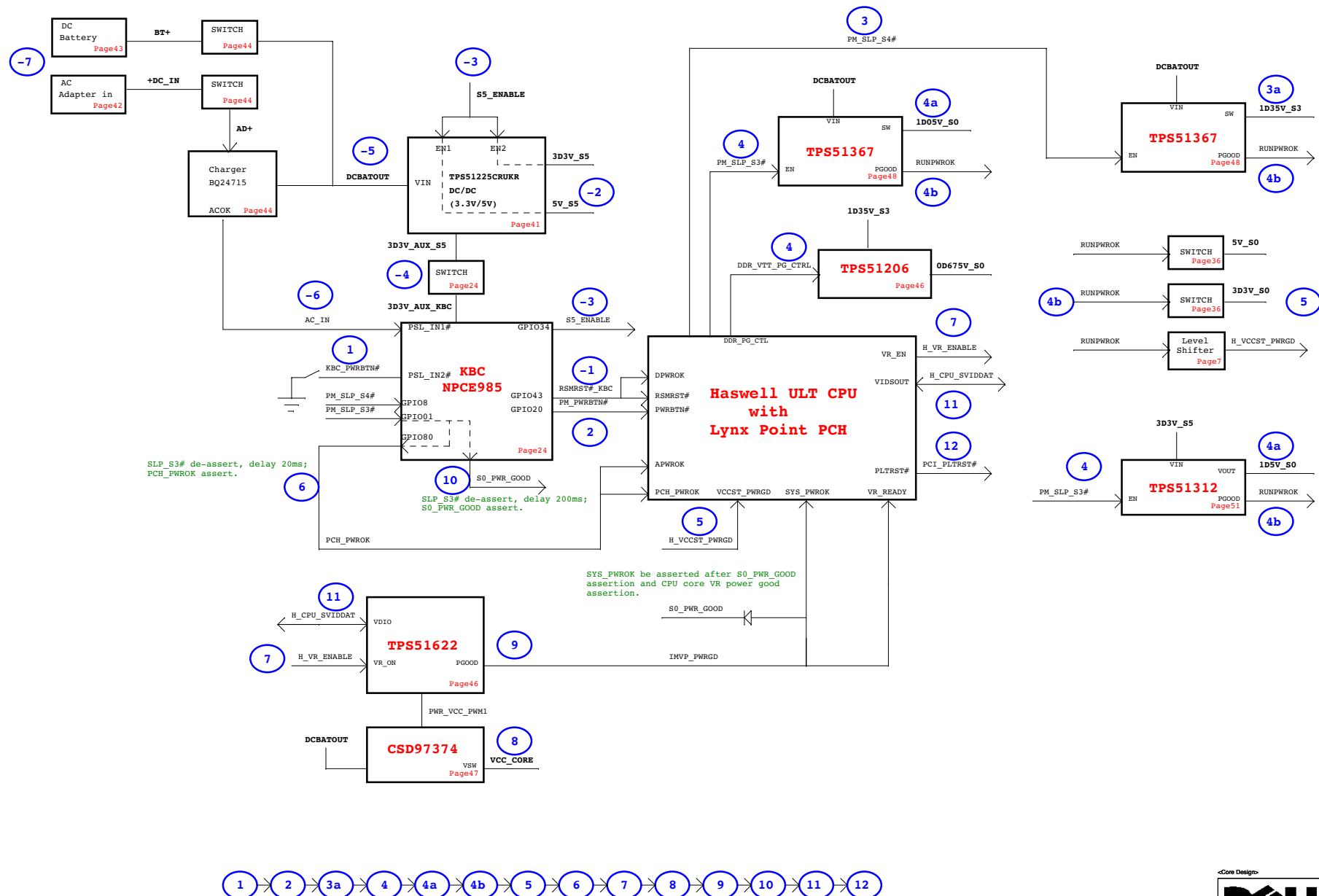


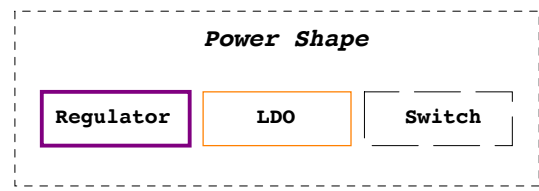
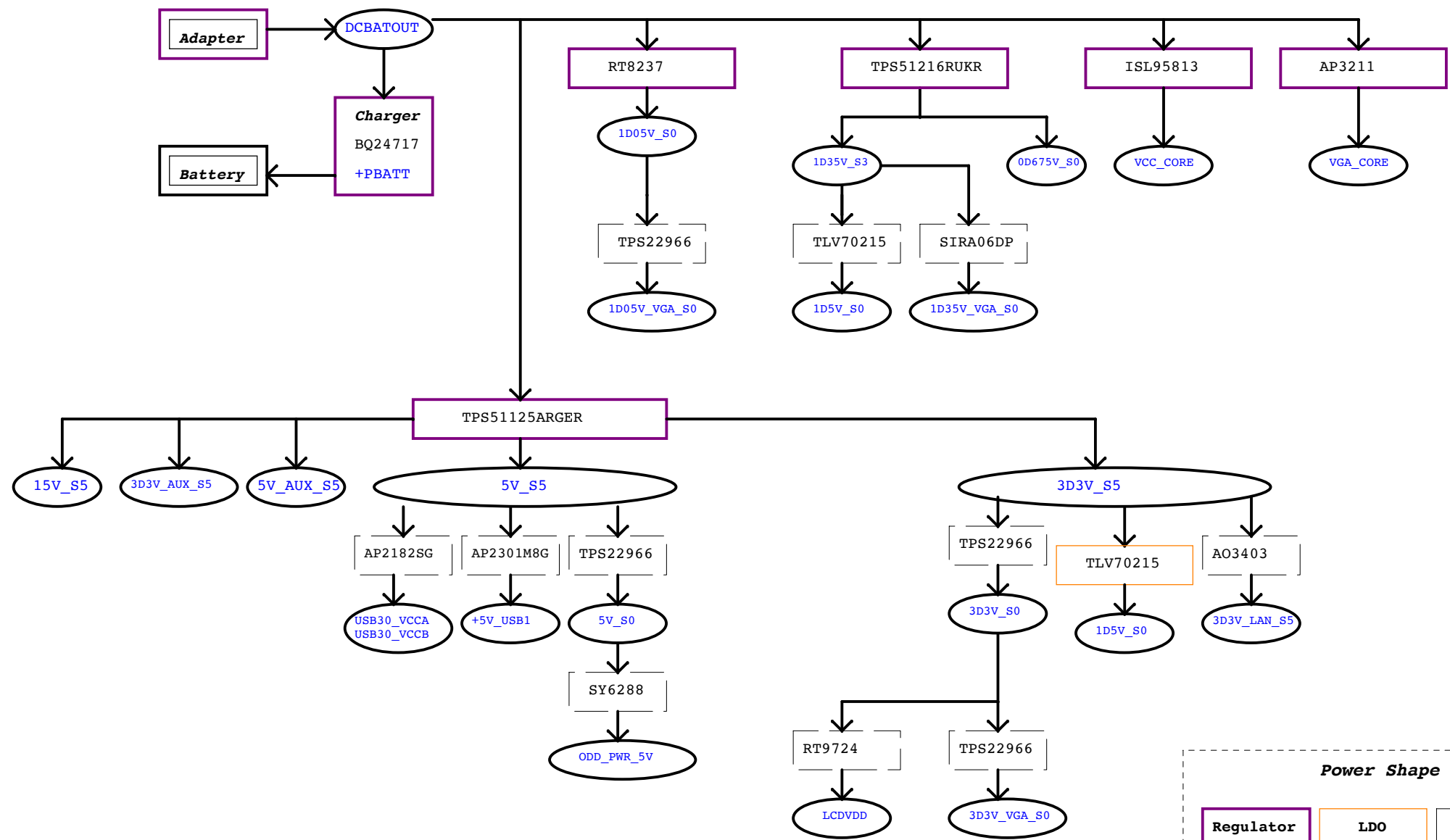
For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

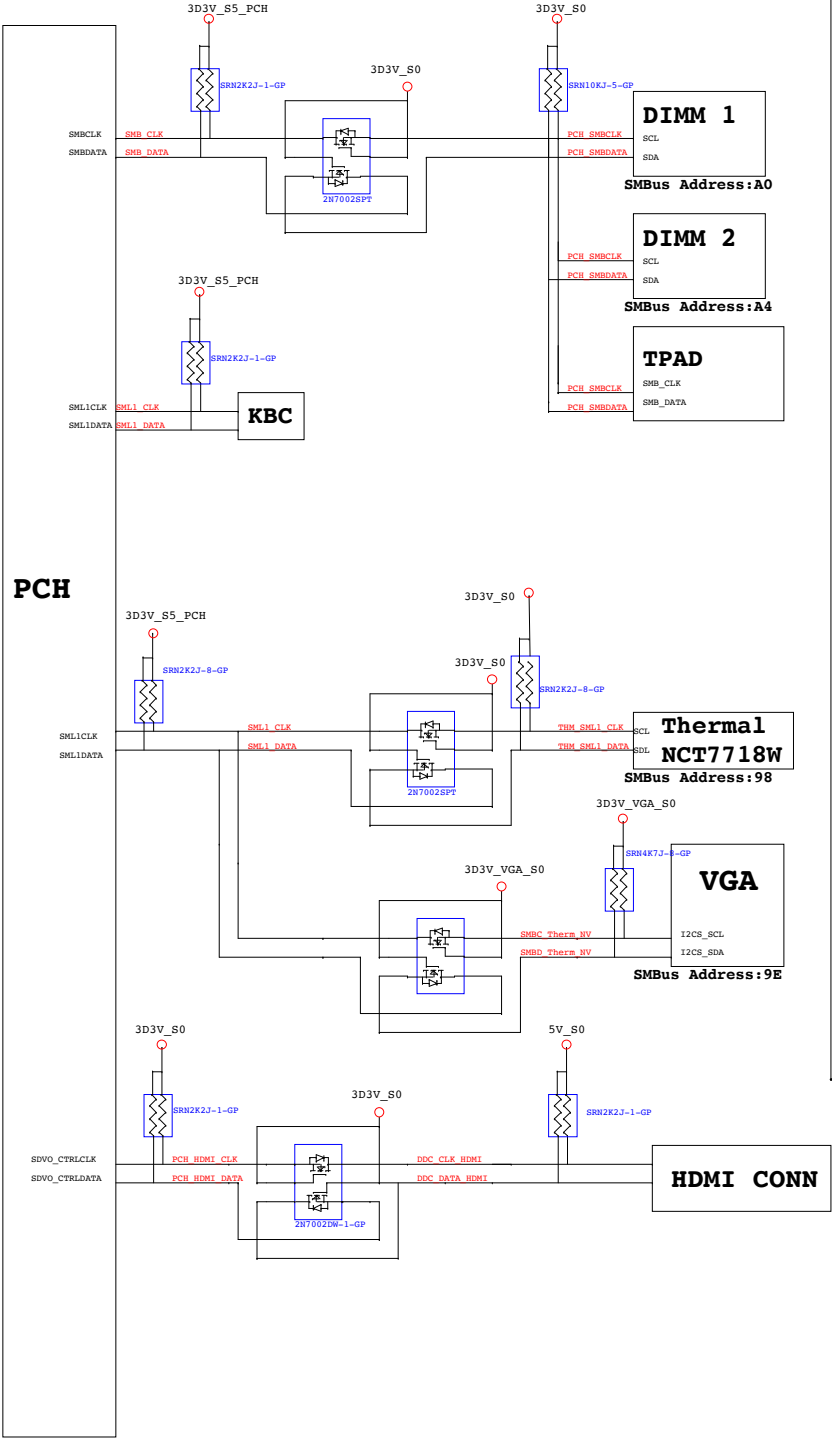


# Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM

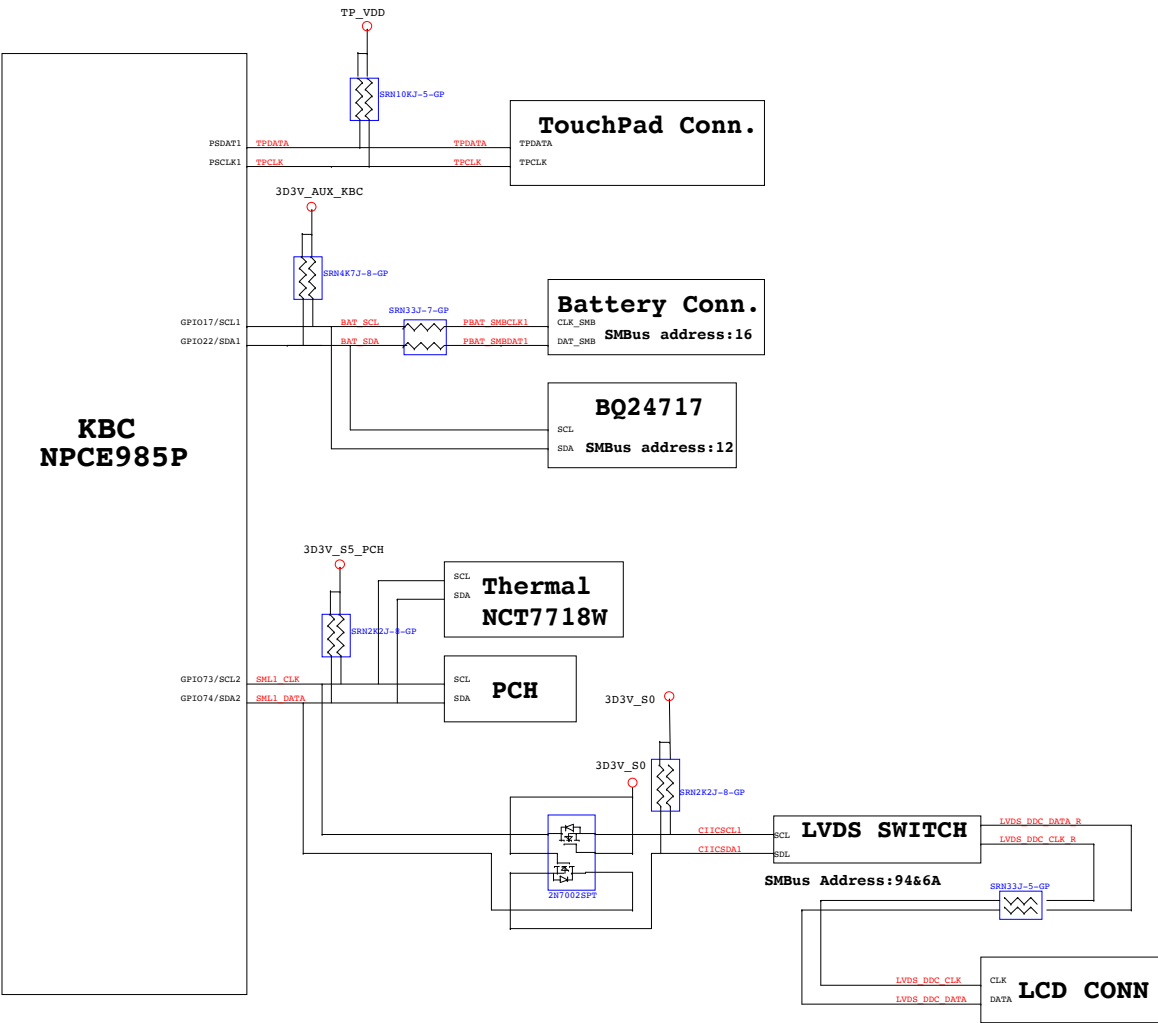




PCH SMBus Block Diagram

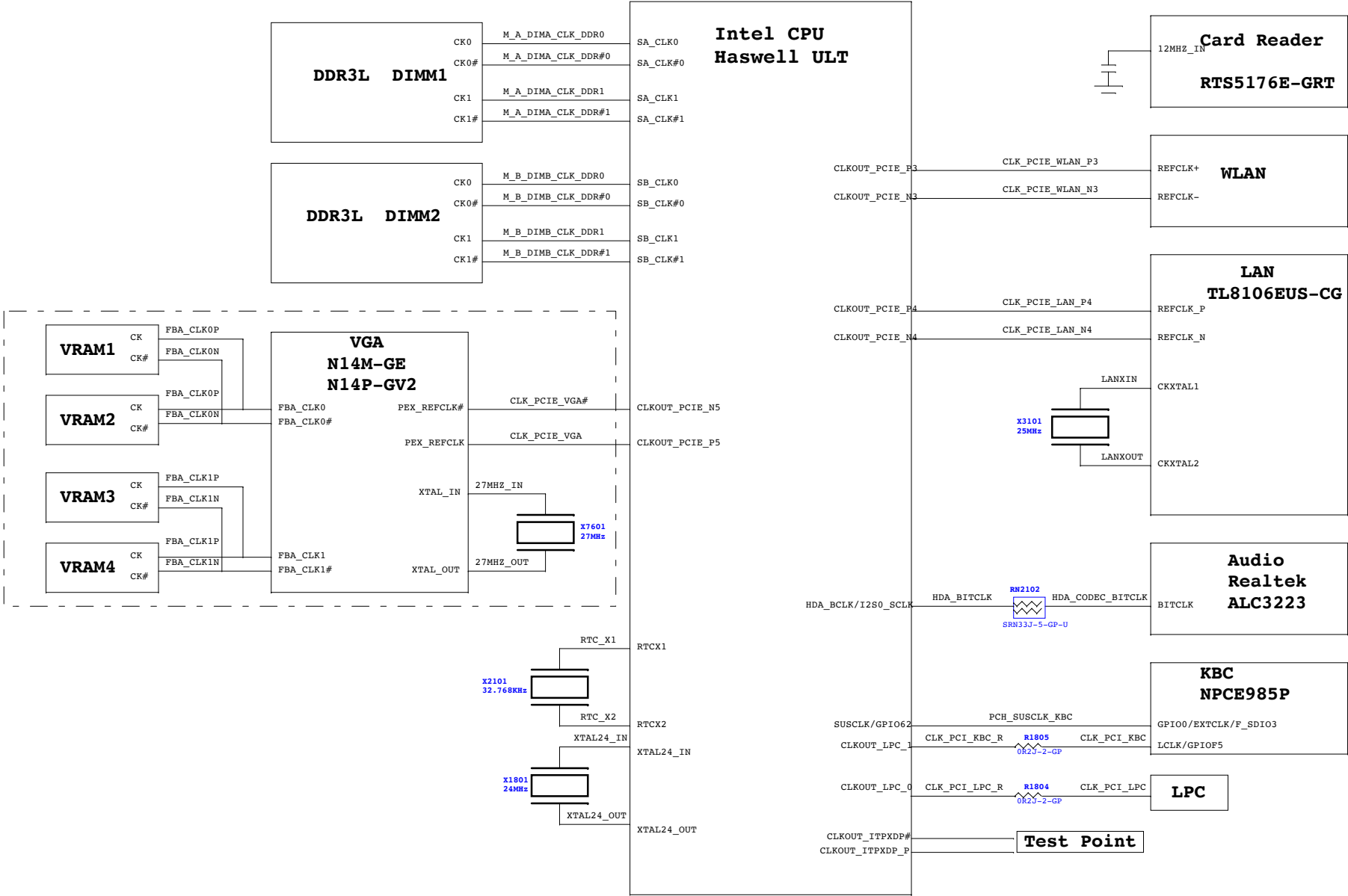


KBC SMBus Block Diagram

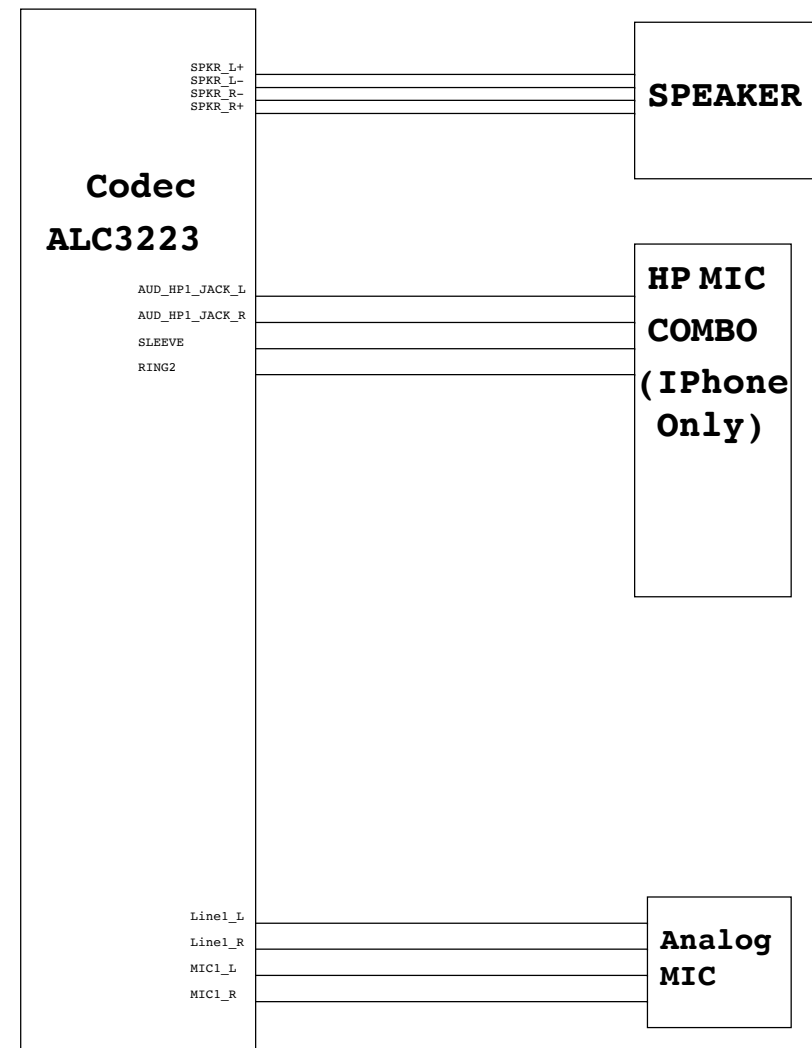


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OAK Haswell CLK Block Diagram




## Audio Block Diagram



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